

LV530 KBL/ SKL Schematics

Kabylake-U

U22 / U2+3e / U42

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
 For the value, it can be read by the number before R. (R means resistor)
 For the tolerance, it can be read from the last letter.
 For the rating, we don't show on the symbol name.
 For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

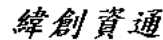
Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
 Capacitor type + value + rating + size + tolerance + material
 SCD1U10V2MX-1
 SC=> SMT Ceremic, TC=> POS cap or SP cap
 D1U => 0.1uF
 10V => the voltage rating is 10V
 2=> 0402, 3=>0603, 5=>0805
 M=>tolerance M, K, Z
 X=> X7R/X5R, Y=> Y5V
 -1 => symbol version, nonsense to EE characteristic

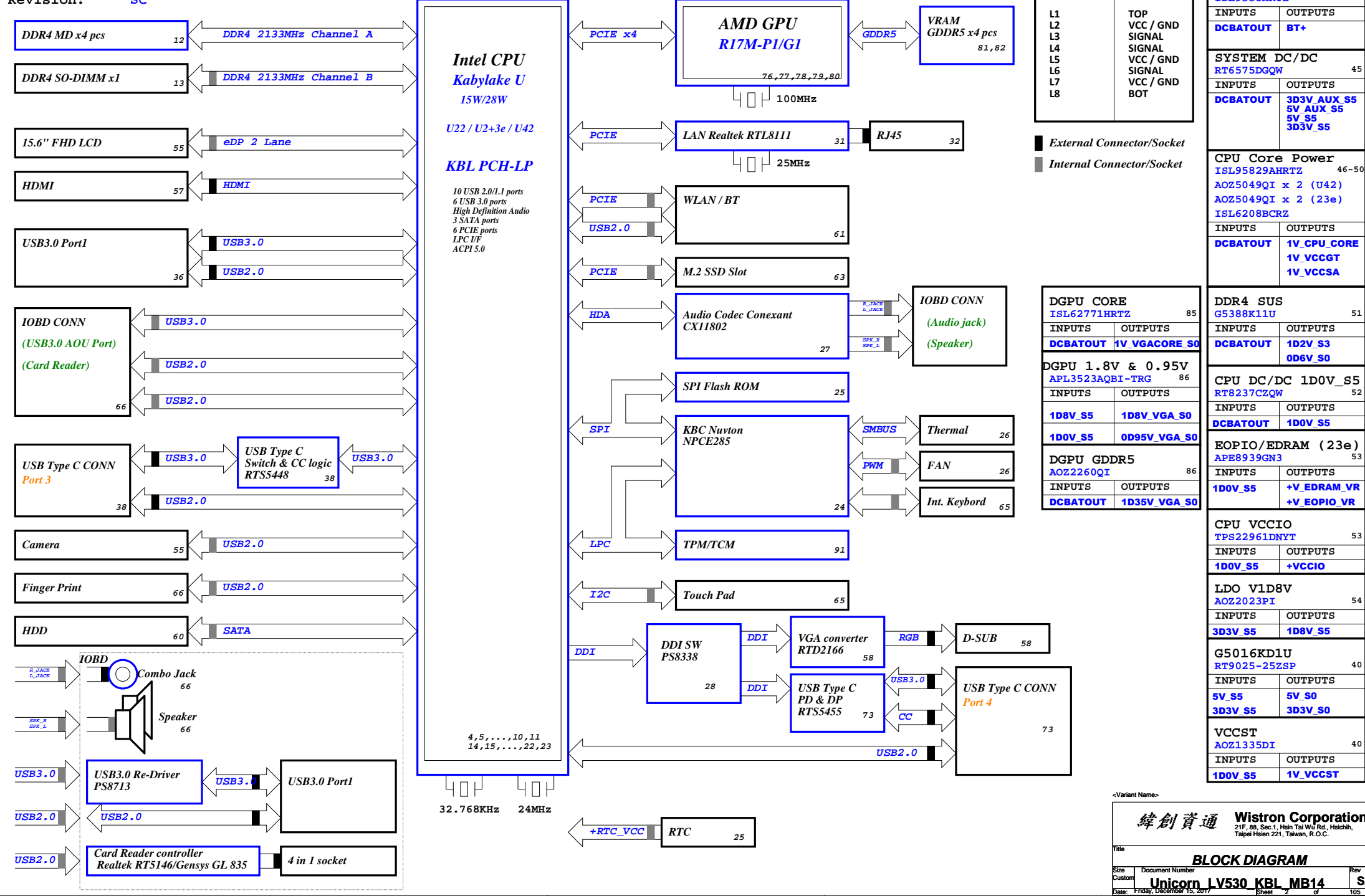
DY	DUMMY
DY-EMC	Follow EMC team request (SDV DY)
EMC-TVS	SDV : ASM FVT&SIT : By SKU (SKU1 DY / SKU2 ASM)
EMC-TEST	For EMC team SDV test (SDV : ASM)

23e	U2+3e only
U42	U42 only
NON-U42	U22 or U2+3e
UMA	UMA only
PX	Discrete only

<Variant Name>

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LV315 KBL-U Block Diagram



L1	TOP
L2	VCC / GND
L3	SIGNAL
L4	SIGNAL
L5	VCC / GND
L6	SIGNAL
L7	VCC / GND
L8	BOT

External Connector/Socket
 Internal Connector/Socket

INPUTS		OUTPUTS	
DCBATOUT		BT+	

SYSTEM DC/DC	
RT6575DGQW	

INPUTS		OUTPUTS	
DCBATOUT		3D3V_AUX_S5	
		5V_AUX_S5	
		5V_S5	
		3D3V_S5	

CPU Core Power	
ISL95829AHRZ	
AOZ5049QI x 2 (U42)	
AOZ5049QI x 2 (23e)	
ISL6208BCRZ	

INPUTS		OUTPUTS	
DCBATOUT		1V_CPU_CORE	
		1V_VCCGT	
		1V_VCCSA	

DDR4 SUS			
G5388K11U			
INPUTS		OUTPUTS	
DCBATOUT		1D2V_S3	
		0D6V_S0	

CPU DC/DC 1D0V_S5			
RT8237CZQW			
INPUTS		OUTPUTS	
1D8V_S5		1D8V_VGA_S0	
1D0V_S5		0D95V_VGA_S0	

EOPPIO/EDRAM (23e)			
APE8939GN3			
INPUTS		OUTPUTS	
1D0V_S5		+V_EDRAM_VR	
		+V_EOPPIO_VR	

CPU VCCIO			
TPS22961DNYT			
INPUTS		OUTPUTS	
1D0V_S5		+VCCIO	

LDO V1D8V			
AOZ2023PI			
INPUTS		OUTPUTS	
3D3V_S5		1D8V_S5	

G5016KD1U			
RT9025-25ZSP			
INPUTS		OUTPUTS	
5V_S5		5V_S0	
3D3V_S5		3D3V_S0	

VCCST			
AOZ1335DI			
INPUTS		OUTPUTS	
1D0V_S5		1V_VCCST	

DGPU CORE			
ISL62771HRTZ			
INPUTS		OUTPUTS	
DCBATOUT		1V_VGACORE_S0	

DGPU 1.8V & 0.95V			
APL3523AQBI-TRG			
INPUTS		OUTPUTS	
1D8V_S5		1D8V_VGA_S0	
1D0V_S5		0D95V_VGA_S0	

DGPU GDDR5			
AOZ2260QI			
INPUTS		OUTPUTS	
DCBATOUT		1D35V_VGA_S0	

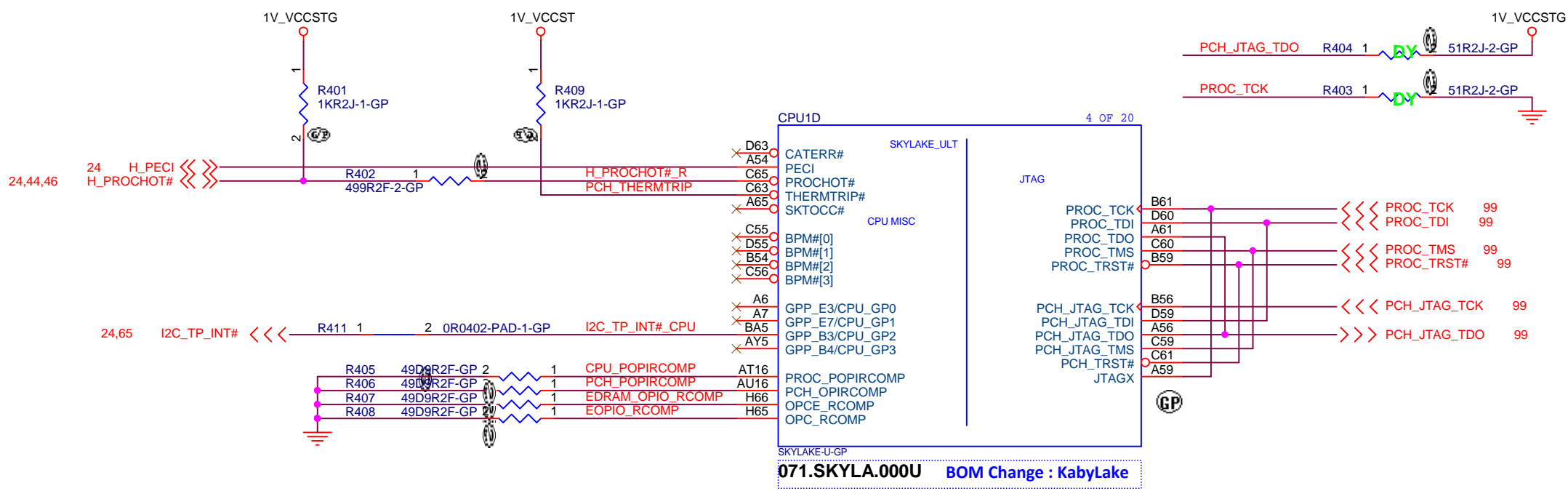
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<Variant Name>

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Size A4	Document Number Unicorn LV530 KBL MB GA	Rev GA
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<Variant Name>

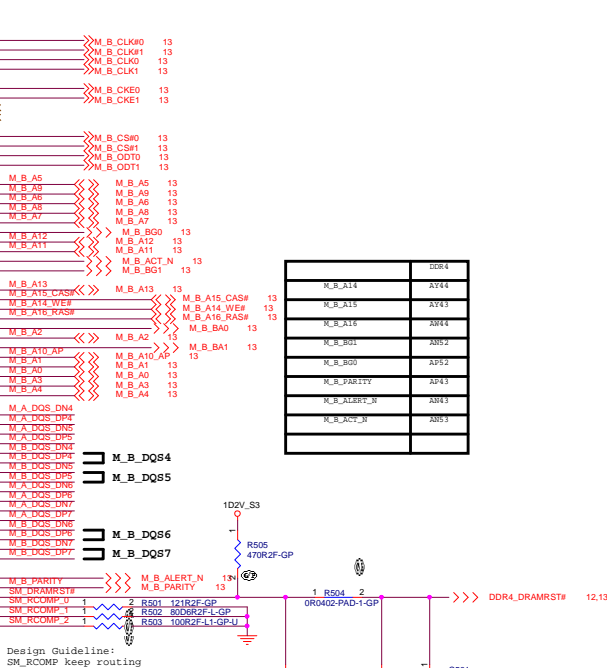
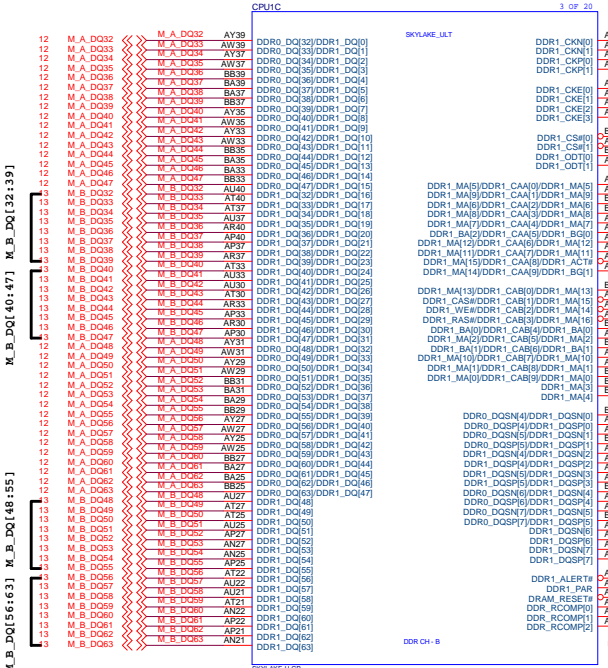
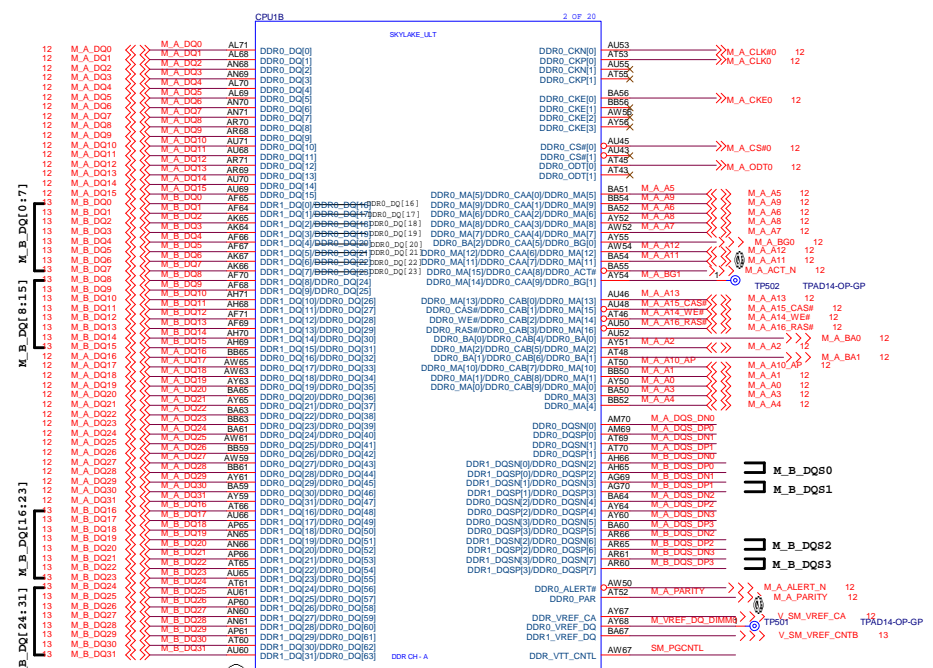
緯創資通 **Wistron Corporation**
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 Taipei Hsien 221, Taiwan, R.O.C.

Title **CPU (JTAG/CPU SIDE BAND)**

Size A4	Document Number Unicorn_LV530_KBL_MB14	Rev SA
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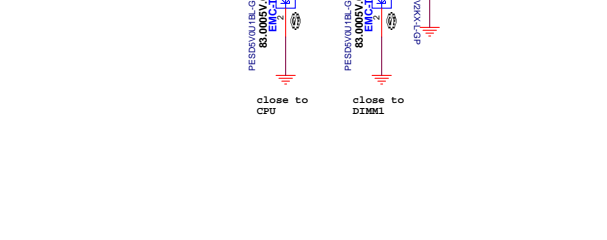
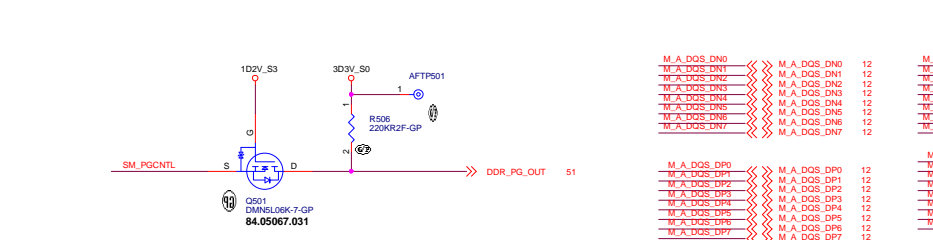
M_A_BGL, M_VREF_DQ_DIMM0 Reserve Testpoint only



071.SKYLA.000 BOM Change : KabyLake

071.SKYLA.000 BOM Change : KabyLake

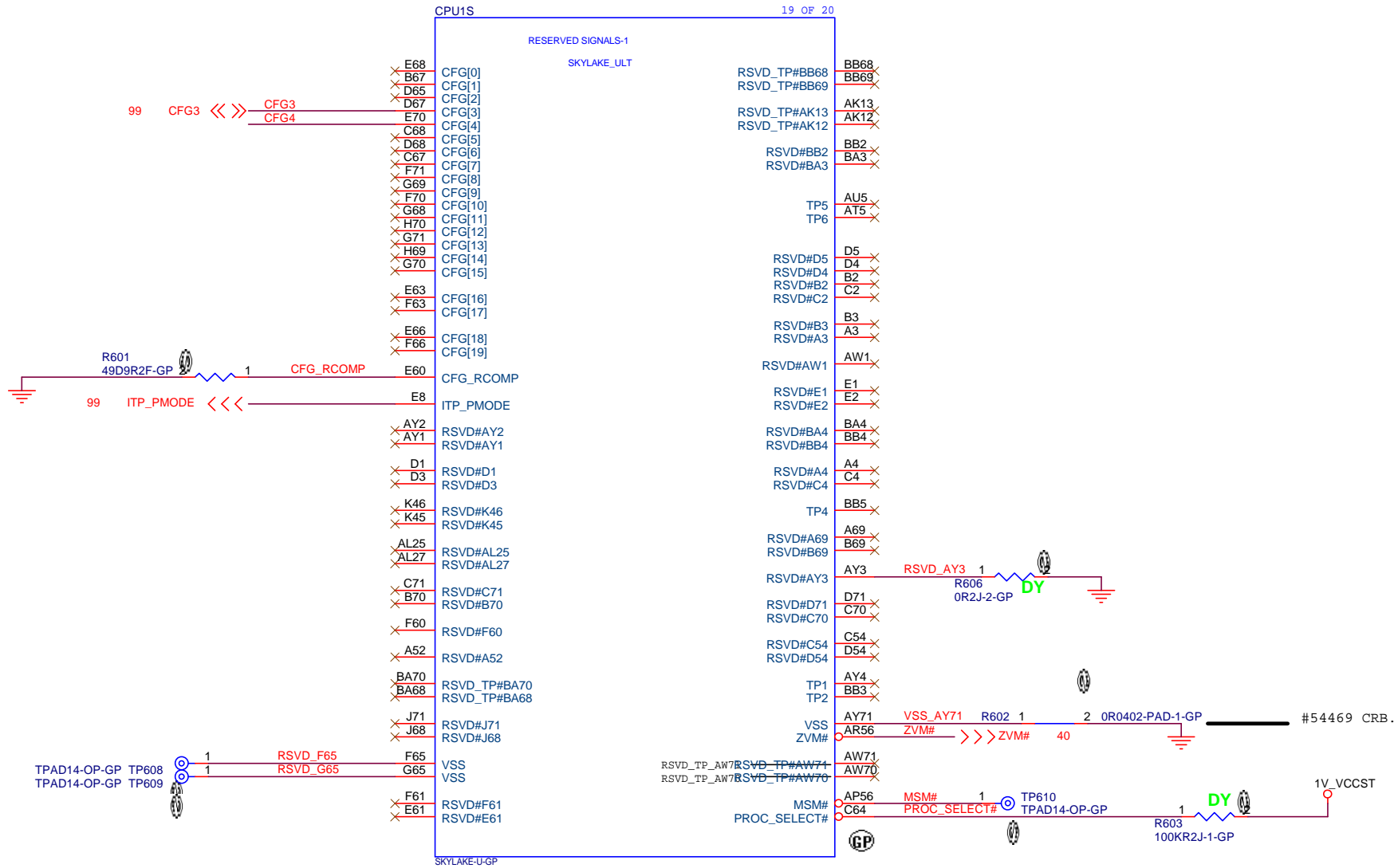
071.SKYLA.000 BOM Change : KabyLake



Design Guideline: SM_RCMP keep routing length less than 500 mils.

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 緯創資通
 21F, 8F, Sec. 1, Hsinchu Rd. East, Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.
 Title: CPU (DDR)
 Docuware Number: Unicorn_LV530_KBL_MB14
 Rev: SA
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Main Func = CPU



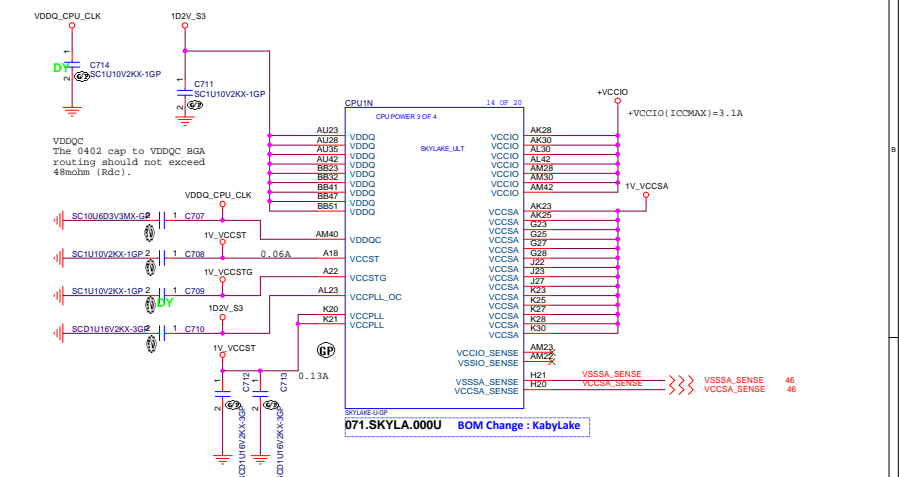
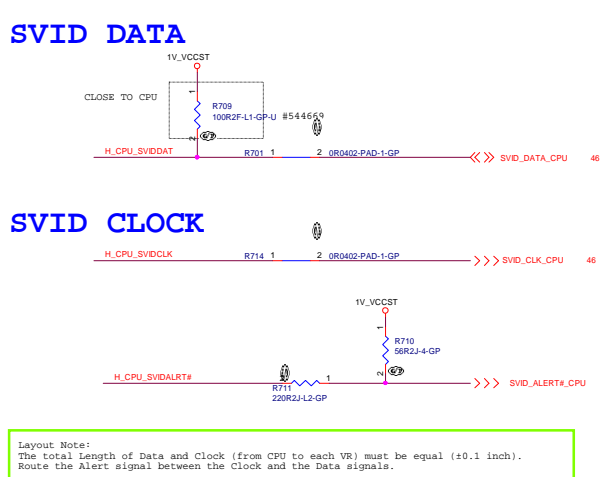
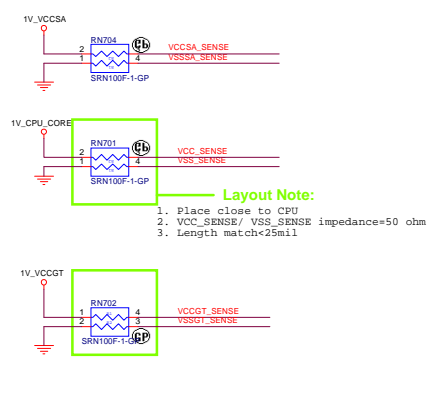
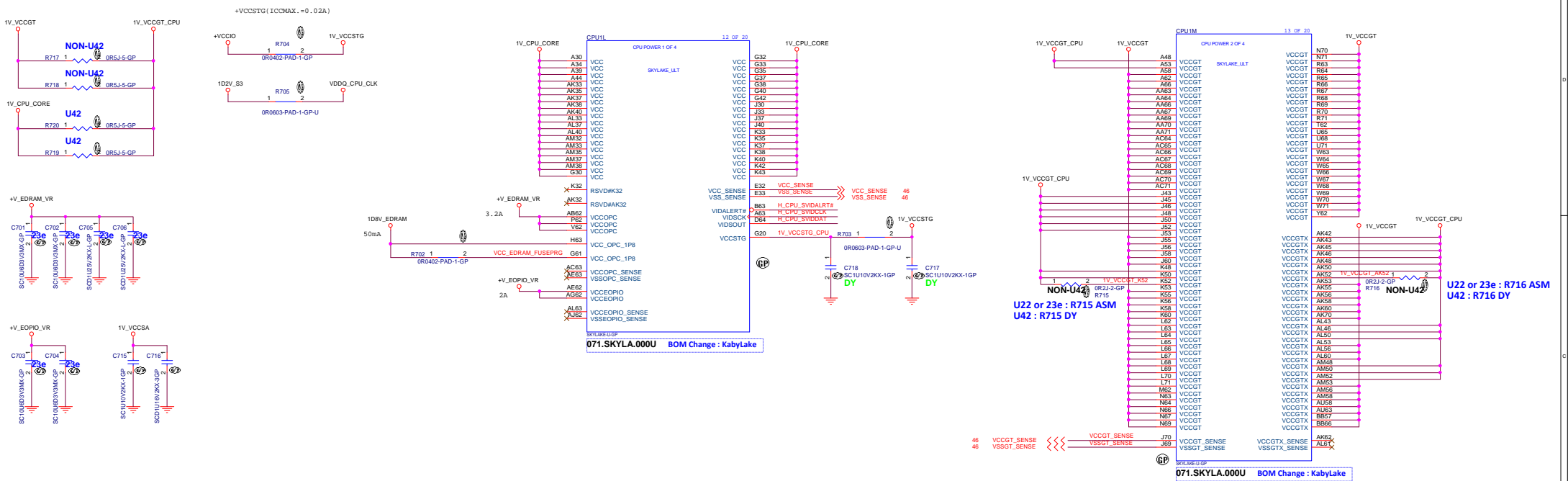
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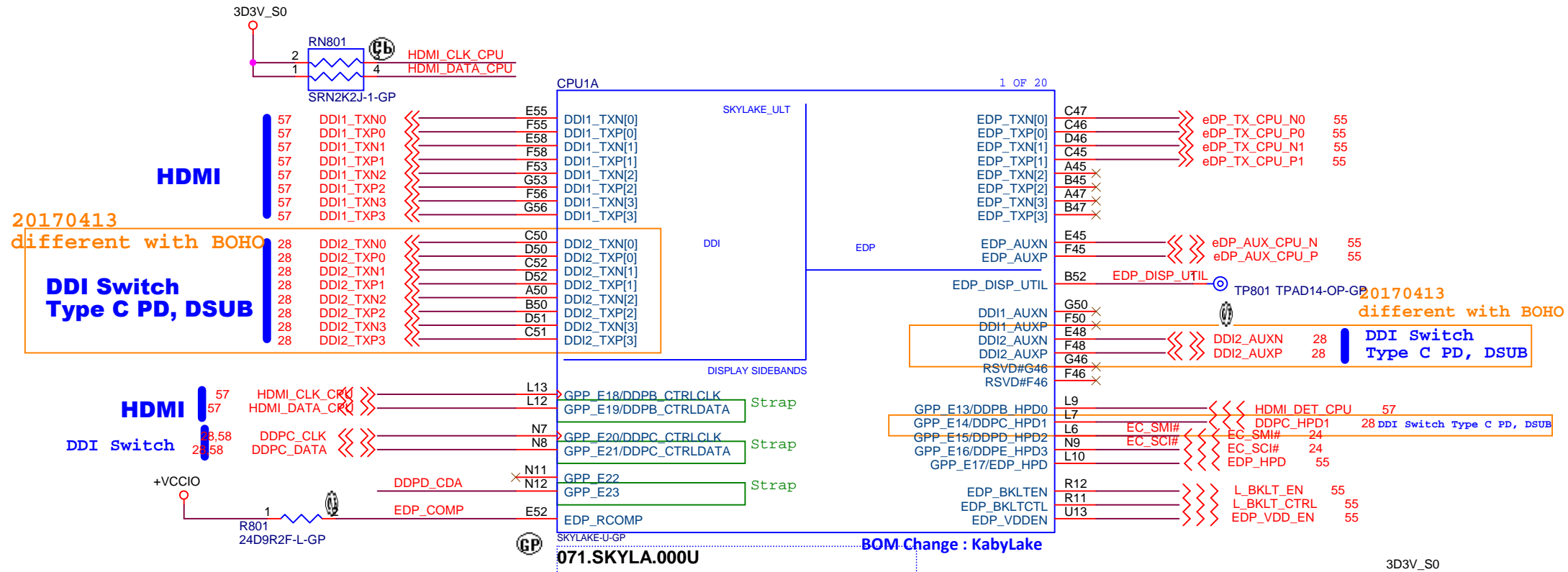
[559100]
 CFG[3]: Reserved configuration lane.
 CFG[4]: eDP enable:
 1 = Disabled.
 0 = Enabled.

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Title		
CPU (CFG)		
Size	Document Number	Rev
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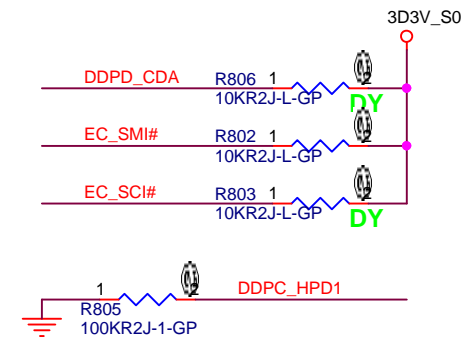


[561280] eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	5 mils	25 mils	24.9 Ω ±1%	Max = 600 mils

[561280] DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC



<Variant Name>

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Title: **CPU (DDI/EDP)**

Size A4 Document Number: **Unicorn LV530_KBL_MB14** Rev: **SA**

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Main Func = CPU

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<Variant Name>

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CPU (RESERVED)

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GT:

U-Line_22/23e

U-line 22/23e 15W/28W
IccMax current-10ms max[A] = 64 A

22uF	PCS	Cap
Suggestion	32	330uF*1 (U22)
Suggestion	32	330uF*2 (U23e)
OPP	26	330uF*1 (U22)

U-Line_42

U-line 22/42 15W/28W
IccMax current-10ms max[A] = 32 A

22uF	PCS	Cap
Suggestion	26	330uF*1

IA:

U-Line_22/23e

U-line 22/23e 15W/28W
IccMax current-10ms max = 32 A

22uF	PCS	Cap
Suggestion	30	330uF*1
OPP	22	330uF*1

U-Line_42

U-line 42
IccMax current-10ms max = 64 A

22uF	PCS	Cap
Suggestion	32	330uF*2

VCCSA:

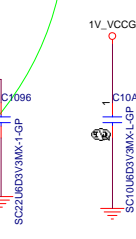
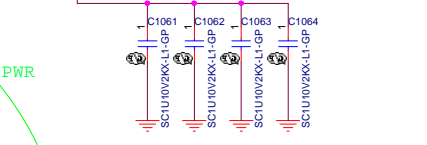
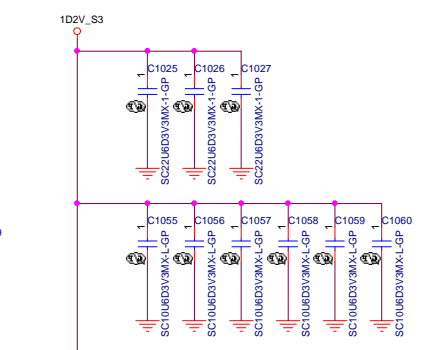
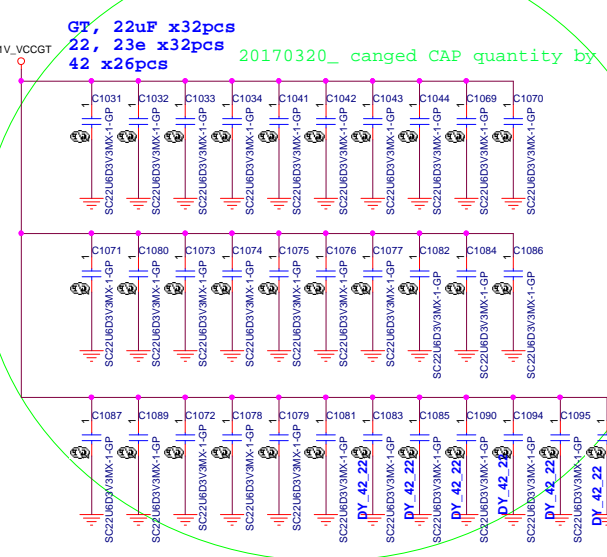
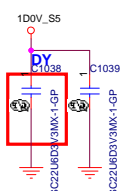
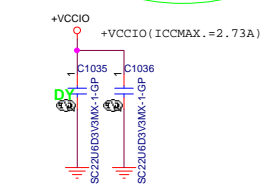
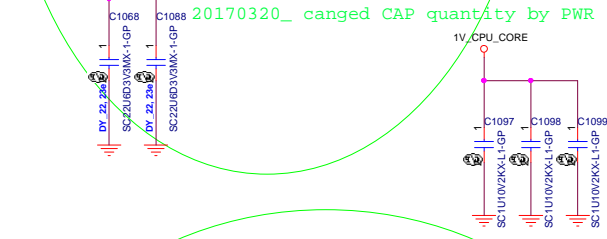
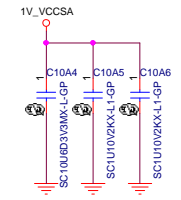
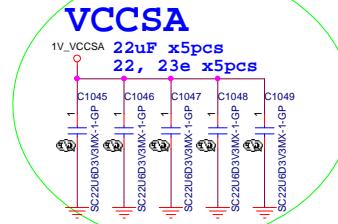
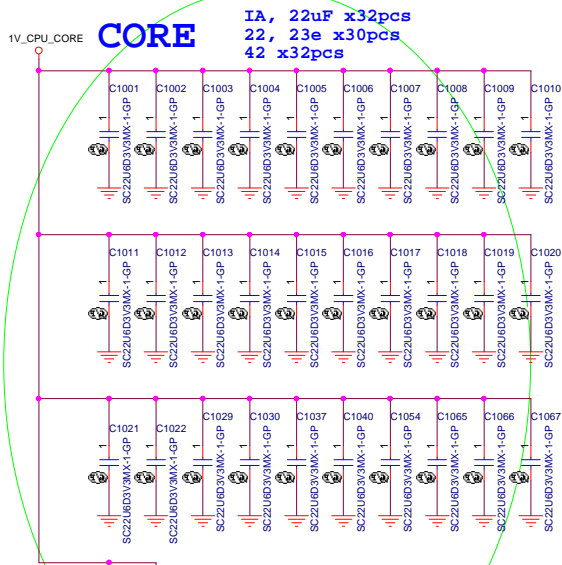
U-Line

U-line 22/23e 15W/28W
IccMax current-10ms max[A] = 5.1 A

22uF	PCS
Suggestion	5
OPP	5

Main Func = CPU

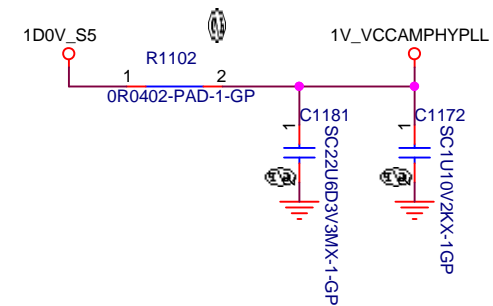
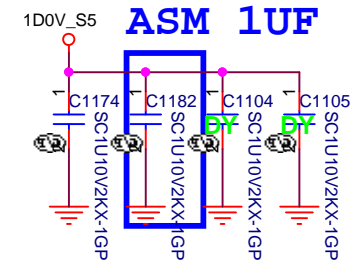
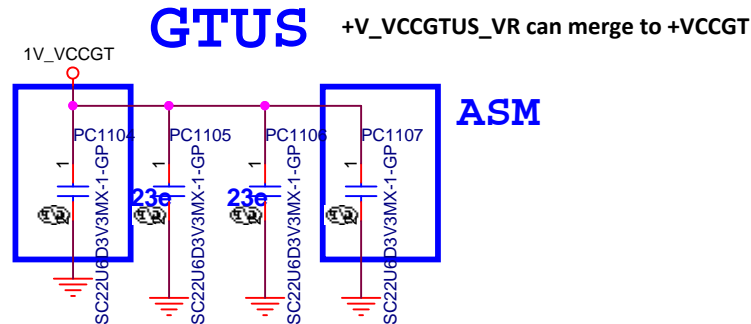
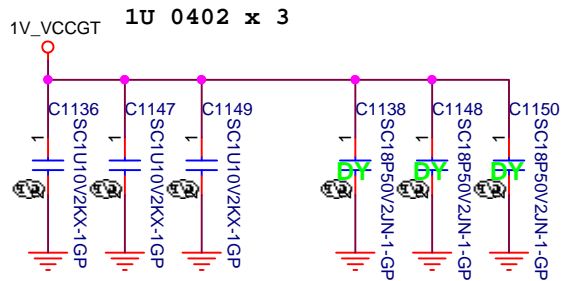
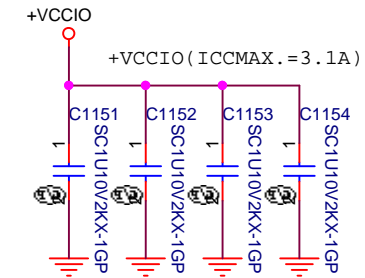
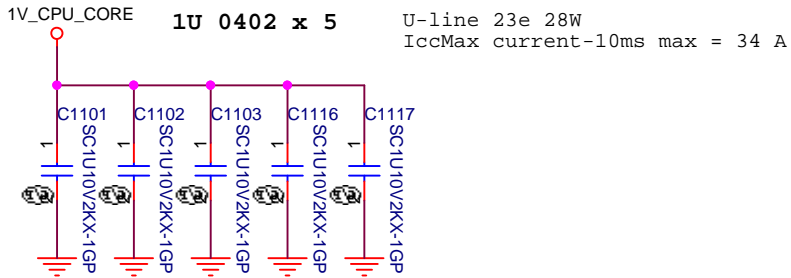
20170320 changed CAP quantity by PWR



<Variant Name>

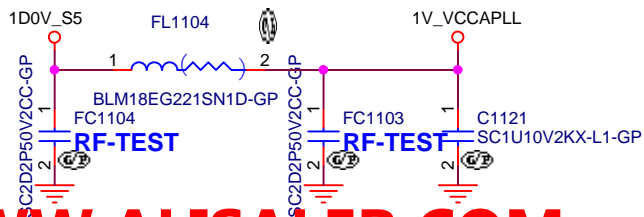
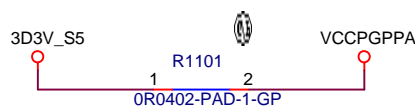
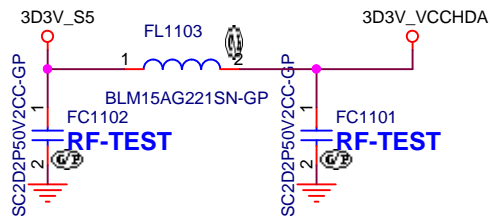
緯創資通 Wistron Corporation	
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CPU (POWER CAP1)	
Size Custom	Document Number Unicorn_LV530_KBL_MB14A
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Main Func = CPU



PCH DERIVED RAILS

VCCPGPPA(ICCMAX.=0.05A)



<Variant Name>

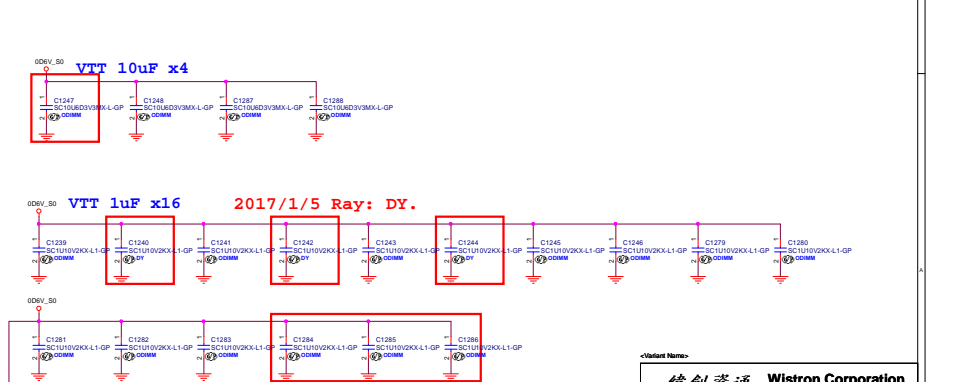
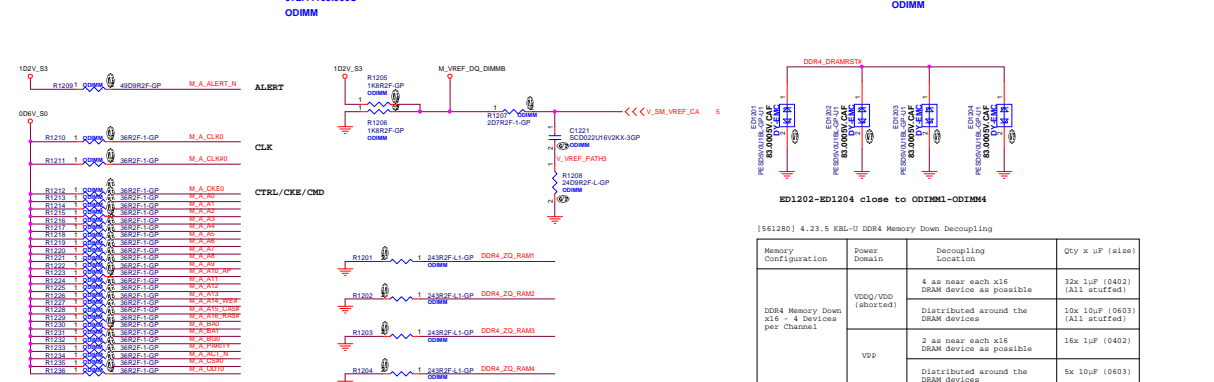
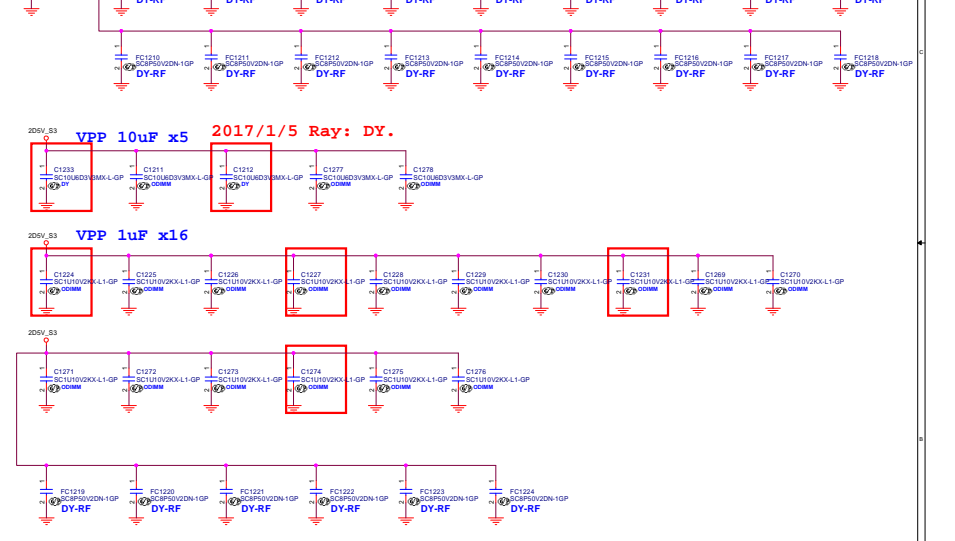
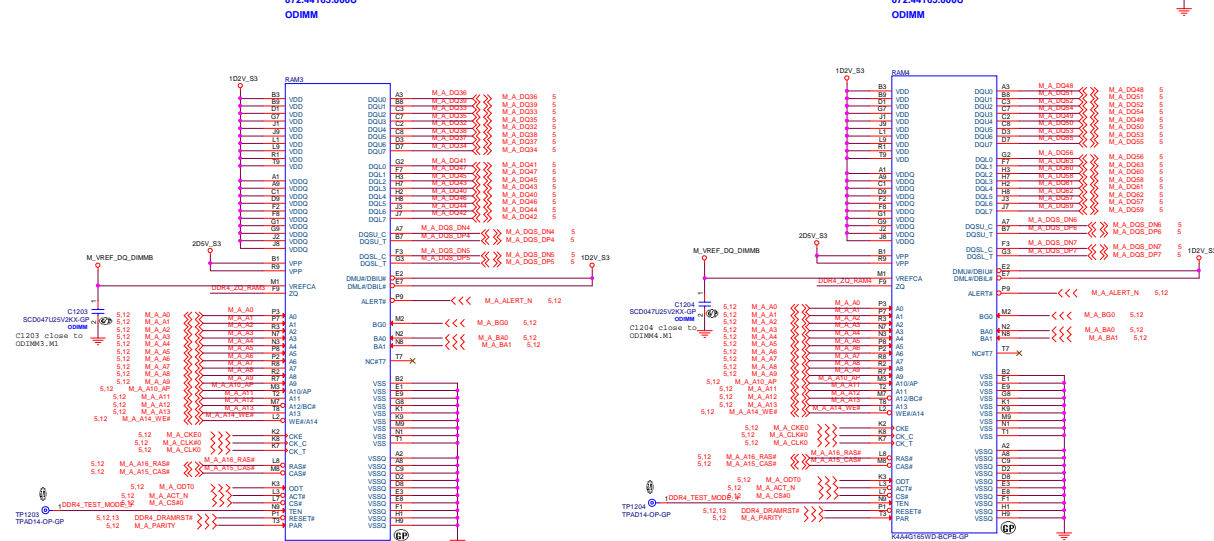
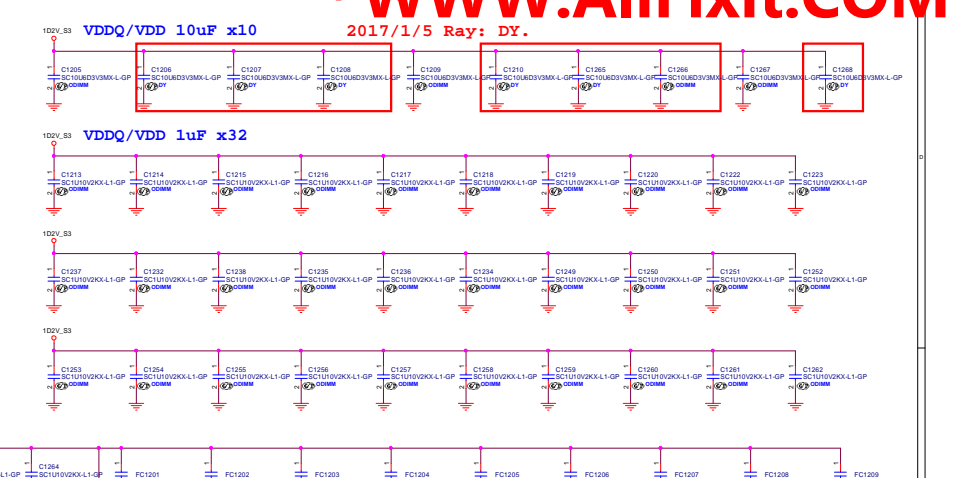
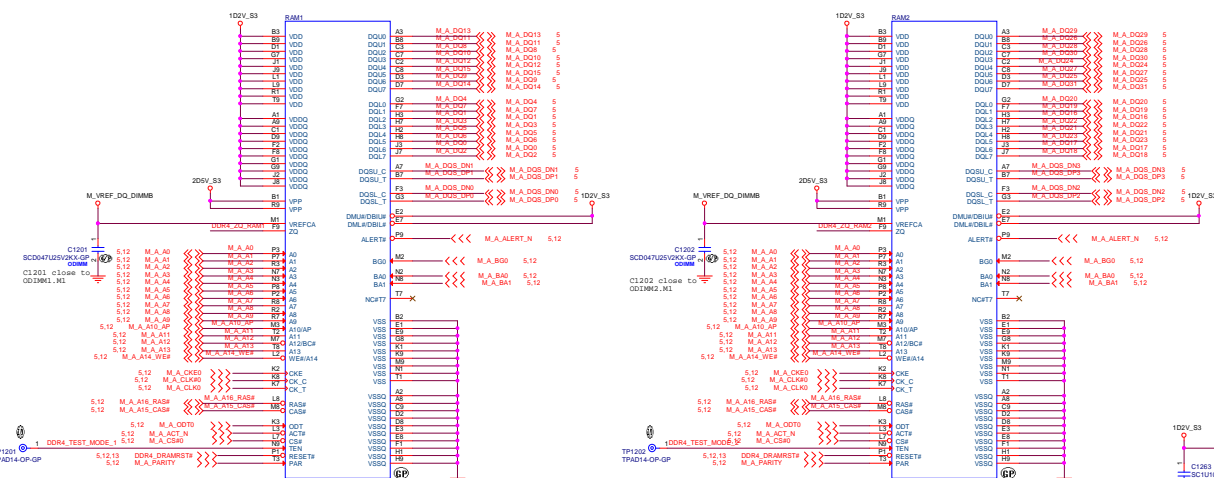
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Title

CPU (POWER CAP2)

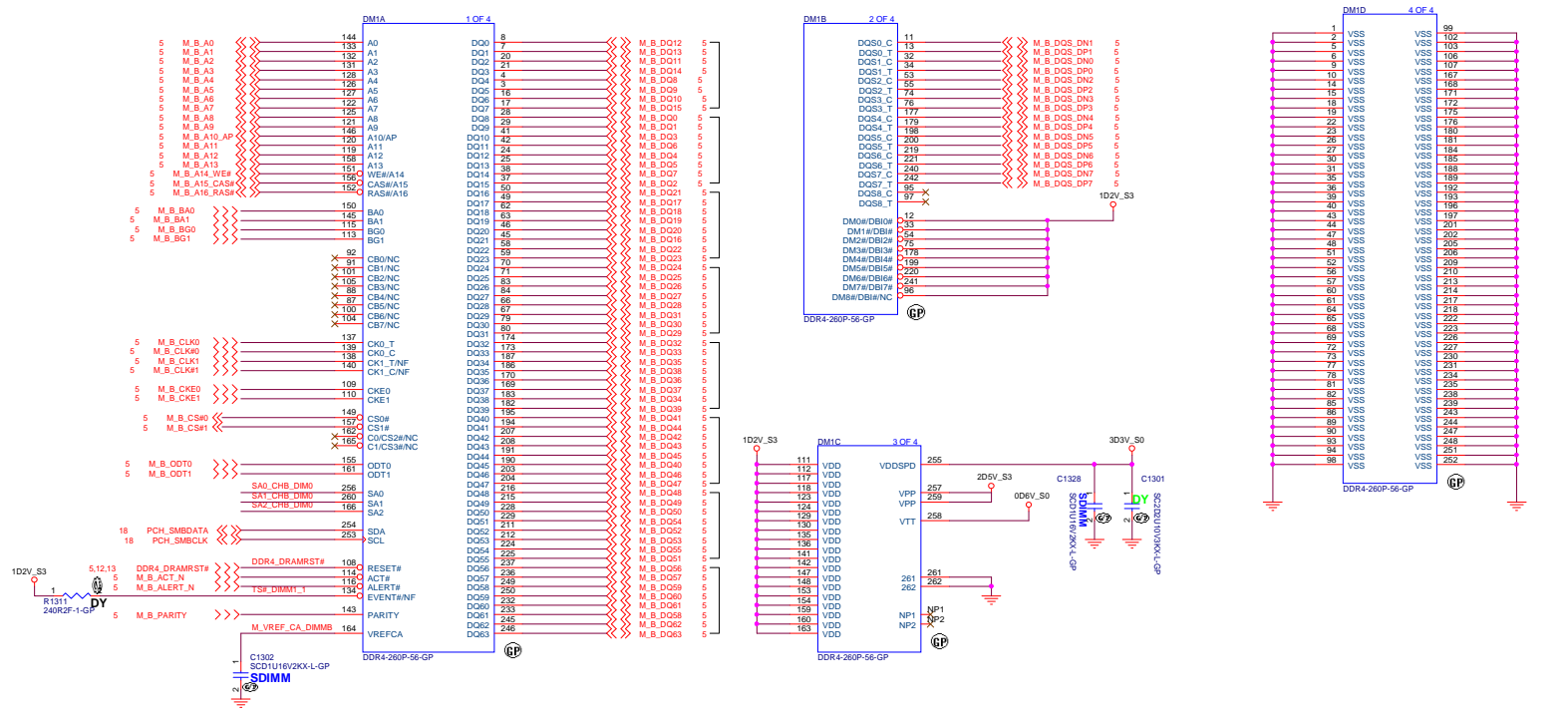
Size A4 Document Number Unicorn_LV530_KBL_MB14 Rev SA

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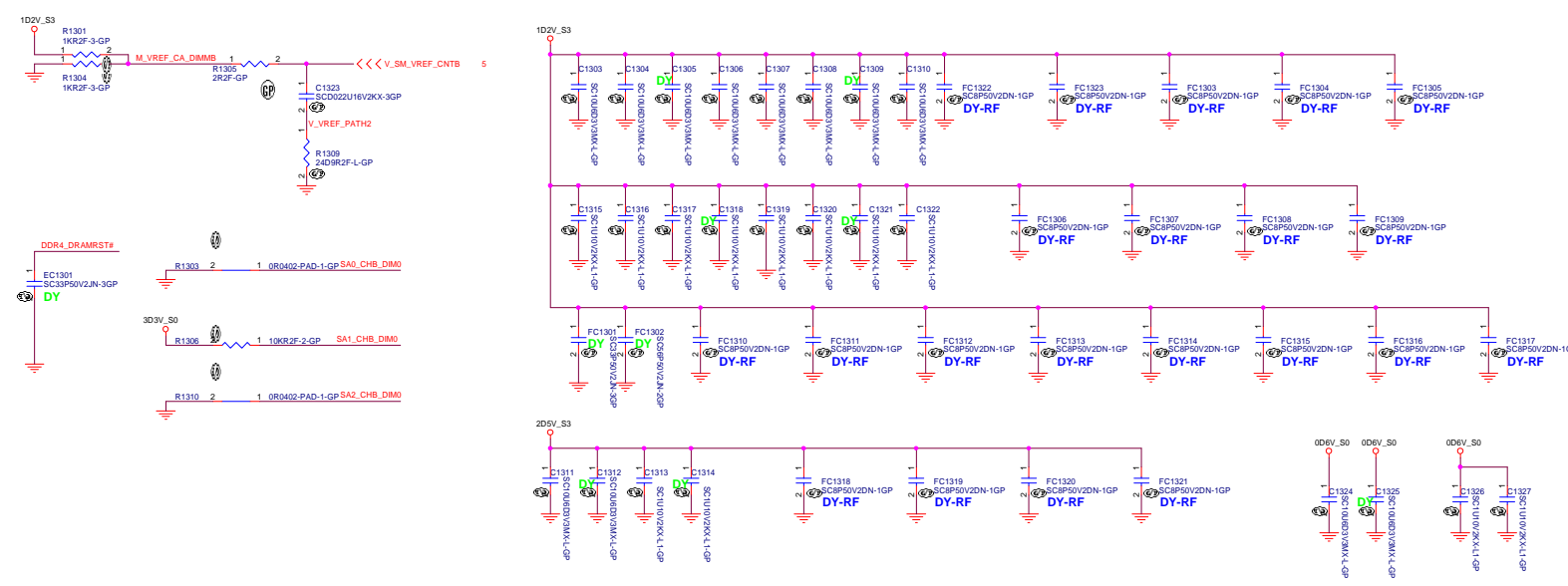


[61280] 4.23.5 KBL-U DDR4 Memory Down Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x uP (size)
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x16 DRAM device as possible	32x 1uF (0402) (All stuffed)
	VDD	Distributed around the DRAM devices	10x 10uF (0603) (All stuffed)
VPP	2 as near each x16 DRAM device as possible	Distributed around the DRAM devices	16x 1uF (0402) 5x 10uF (0603)
	VTT	2 as near each x16 DRAM device as possible	16x 1uF (0402) 4x 10uF (0603)



12/09 Ray
Need to check property



[561280] 4.23.6 KBL~DDR4 SODIMM Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)
DDR4 SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10 μ F (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1 μ F (0402)
	VTT	1 placeholder	1x 330 μ F (7343)
		Place these caps on the VTT plane close to SODIMM	1x 10 μ F (0805)
	VPP	Place these caps on the VTT plane close to SODIMM	1x 10 μ F (0402)
		Place these caps on the VTT plane close to SODIMM	4x 1 μ F (0402)
	VDDSPD	DRAM Side	2x 10 μ F (0603)
		DRAM Side	2x 1 μ F (0402)
		Place close to DIMM	1x 0.1 μ F (0402)
		Place close to DIMM	1x 2.2 μ F (0402)

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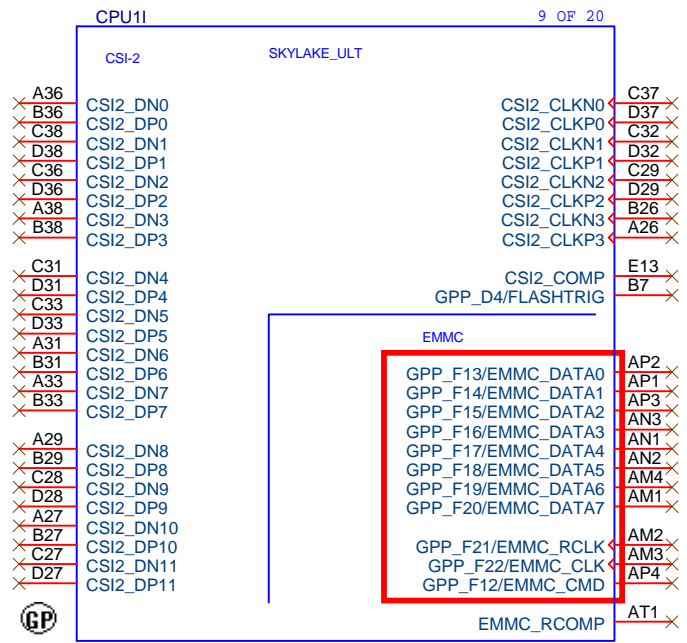
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Title	RESERVED
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Size A4	Document Number Unicorn LV530 KBL MB GA	Rev GA
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GPP_F: VCCPGPPF = 1.8V Only

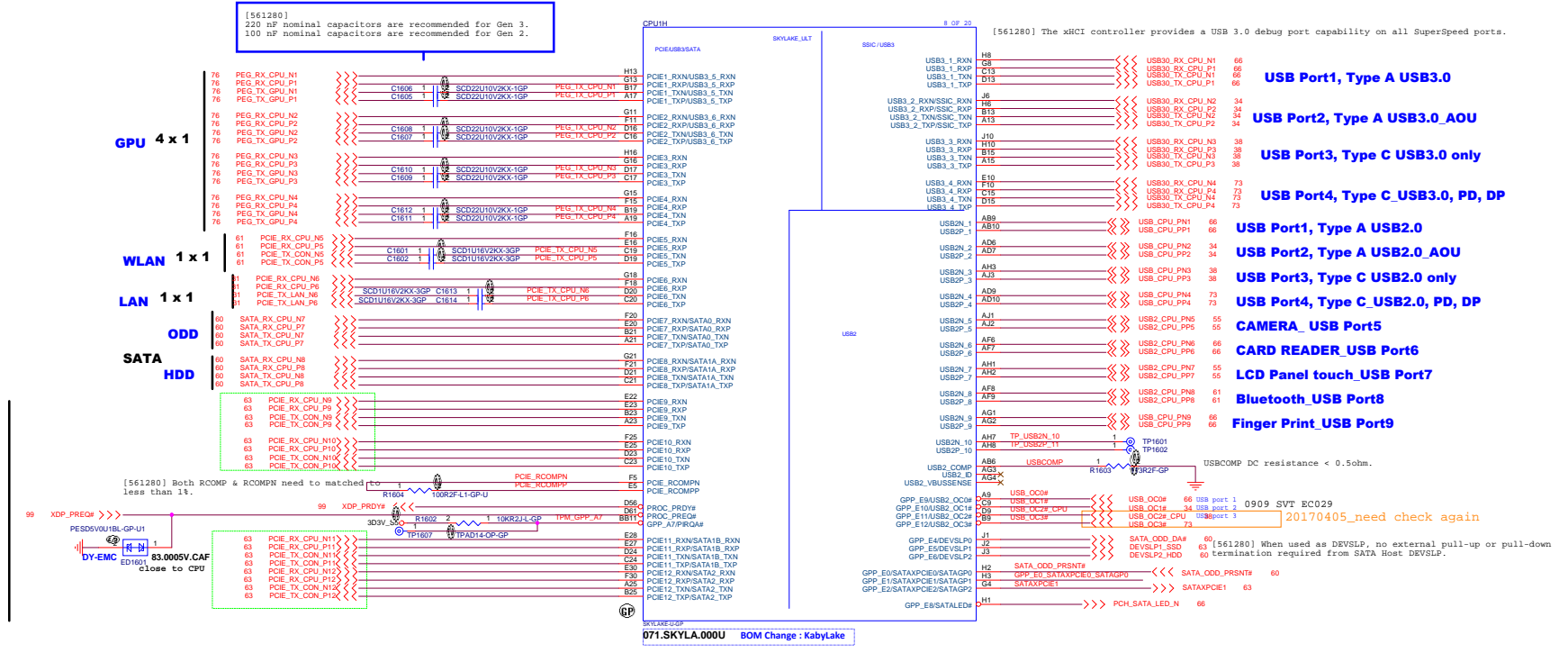
071.SKYLA.000U BOM Change : KabyLake

<Variant Name>

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Title: CPU (CSI2/EMMC)

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M.2 SSD Optane
PCIe only

M.2 SSD Optane
PCIe/ SATA

4 x 1

Share SATA

PCIe Table

Port	PCIe Device	Share BUS
1	GPU L0	
2	GPU L1	
3	GPU L2	
4	GPU L3	
5	M.2 SSD	
6	M.2 SSD	
7	M.2 SSD	SATA0
8	M.2 SSD	SATA1A
9	LAN	
10	WLAN	
11	ODD	SATA1B
12	HDD	SATA2

SATA Table

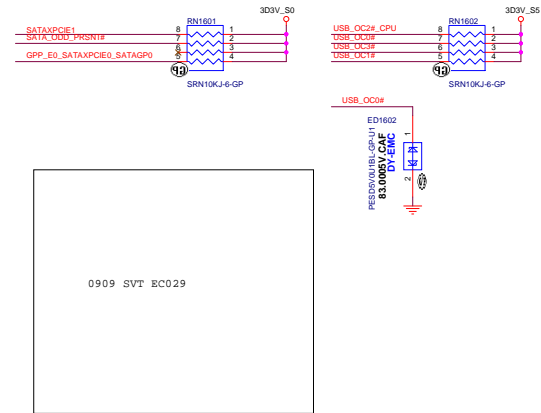
Pair	SATA Device	Share BUS
0	ODD	PCIe7
1A	HDD	PCIe8
1B	M.2 SSD	PCIe11
2	M.2 SSD	PCIe12

USB 3.0 Table

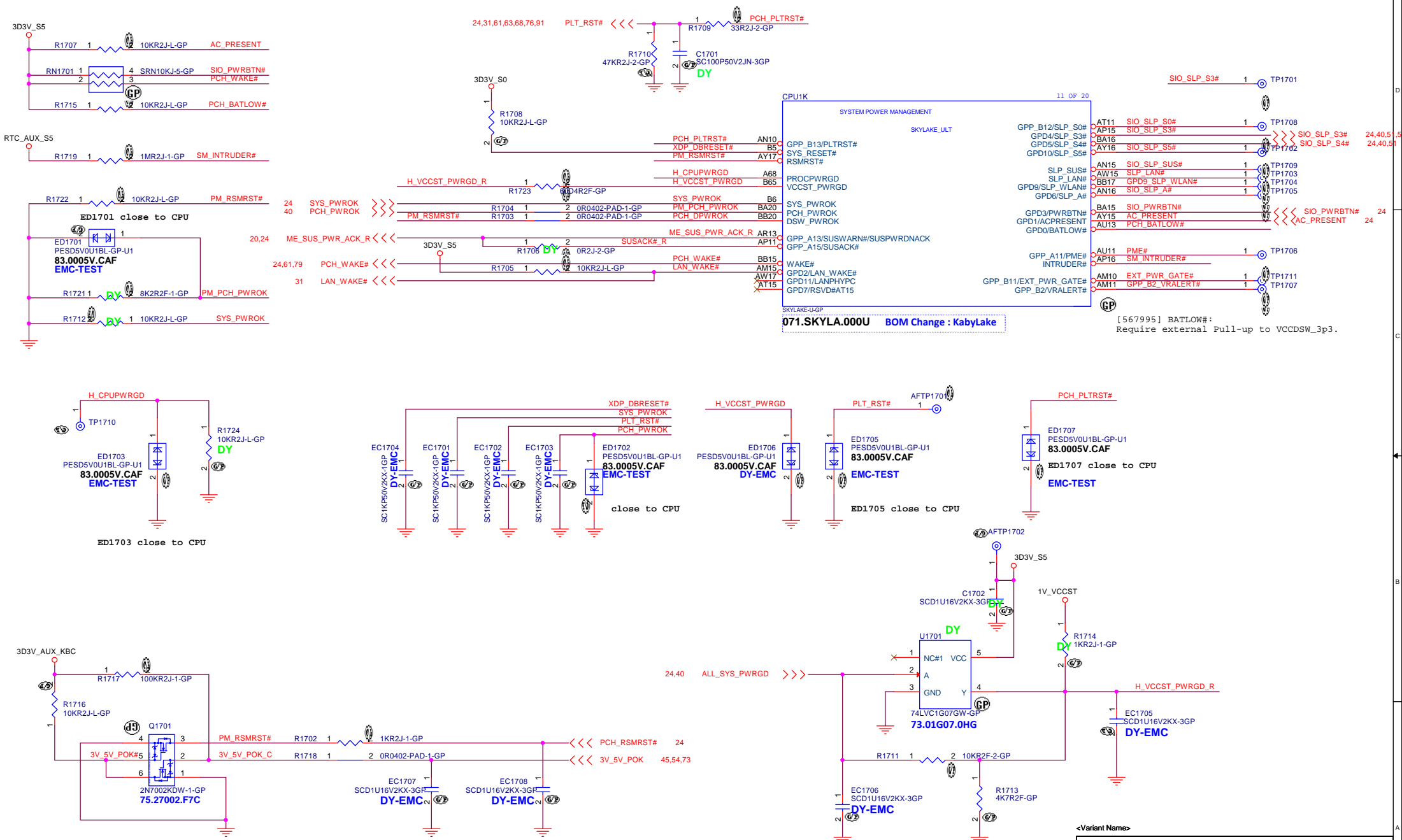
Pair	USB3.0 Device	Share BUS
1	USB3.0 port1 (Type A USB3.0)	
2	USB3.0 Port2 (Type A USB3.0_AOU)	
3	USB Port3, Type C USB3.0 only	
4	USB Port4, Type C, USB3.0, PD, DP	
5	N/A	PCIe1 (GPU)
6	N/A	PCIe2 (GPU)

USB 2.0 Table

Pair	USB2.0 Device
1	USB Port1, Type A USB2.0
2	USB Port2, Type A USB2.0_AOU
3	USB Port3, Type C USB2.0 only
4	USB Port4, Type C, USB2.0, PD, DP
5	CAMERA_USB Port5
6	CARD READER_USB Port6
7	LCD Panel touch_USB Port7
8	Bluetooth_USB Port8
9	Finger Print_USB Port9
10	Ultray bay_USB Port10



Main Func = PCH



<Variant Name>

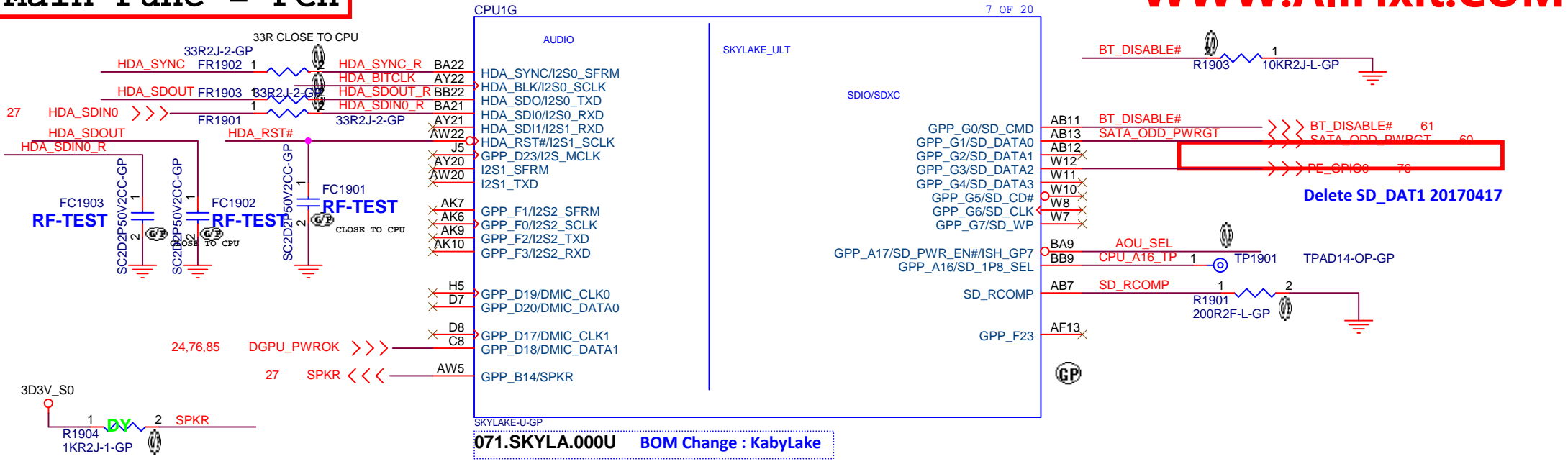
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (PM)**

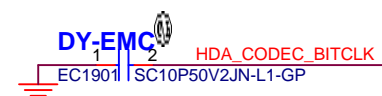
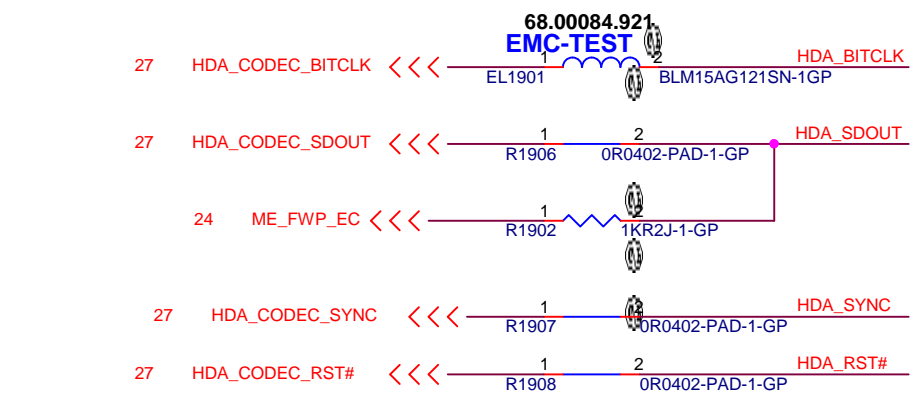
Size A3 Document Number: **Unicorn LV530_KBL_MB13A** Rev: 13A

Date: Friday, December 15, 2017 Sheet 17 of 105

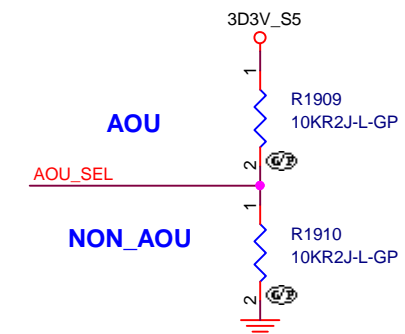
Main Func = PCH



SPKR/GPP_B14
Usage: Top Swap Override
When Sampled: Rising edge of PCH_PWROK
The signal has a weak internal Pull-down.
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.
The internal Pull-down is disabled after PCH_PWROK de-asserts.
This signal is in the primary well.



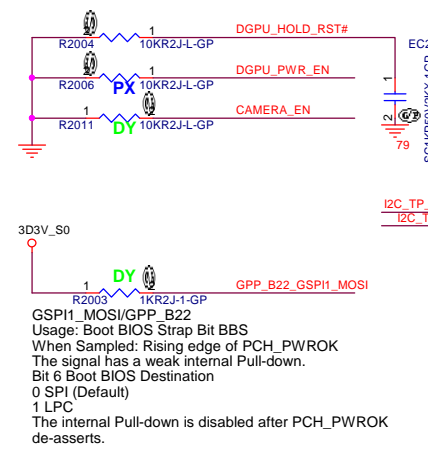
HDA_SDO /I2S_TXD0
Usage: Flash Descriptor Security Override
When Sampled: Rising edge of PCH_PWROK
The signal has a weak internal Pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.
The internal Pull-down is disabled after PCH_PWROK de-asserts.



<Variant Name>

<p>緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>Title</p> <p align="center">CPU (HDA/SDIO/SDXC)</p>		
Size	Document Number	Rev
A4	Unicorn LV530_KBL_MB14	SA
Date:	Friday, December 15, 2017	Sheet 19 of 105

Main Func = PCH

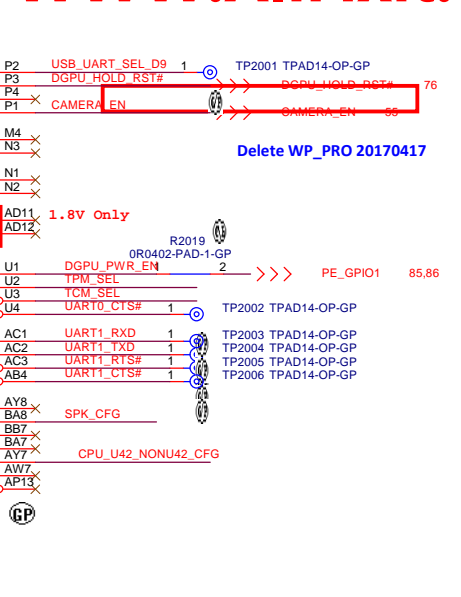
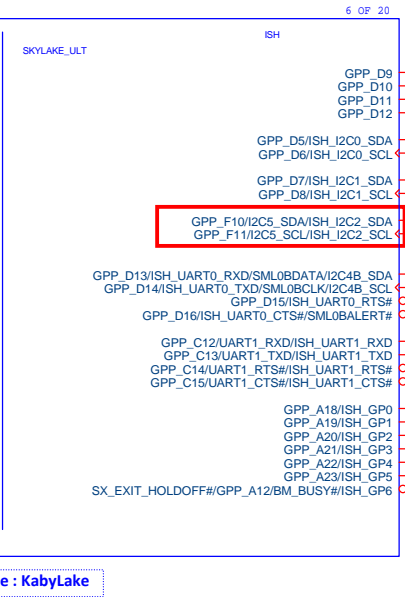
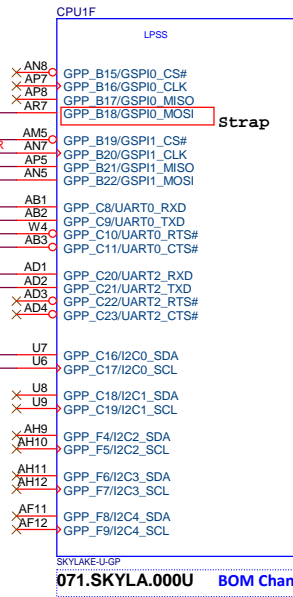


GSP11_MOSI/GPP_B22
Usage: Boot BIOS Strap Bit BBS
When Sampled: Rising edge of PCH_PWROK
The signal has a weak internal Pull-down.
Bit 6 Boot BIOS Destination
0 SPI (Default)
1 LPC
The internal Pull-down is disabled after PCH_PWROK de-asserts.

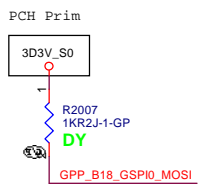
Delete TCM_DET_N 20170417

20170328 added by EE
that is for R16M
RTC_DET#
VIDEO_THERM_ALERT#
TOUCH_RST#

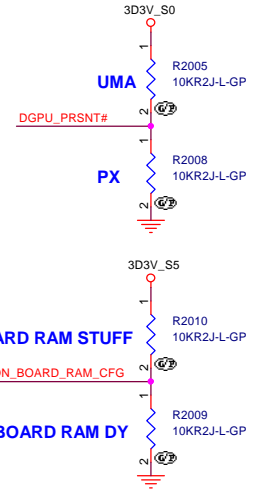
I2C_TP_DATA
I2C_TP_CLK



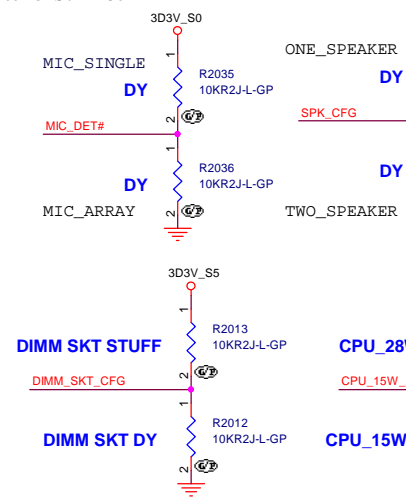
GSP11_MOSI/GPP_B18
Usage: No Reboot
When Sampled: Rising edge of PCH_PWROK
The signal has a weak internal Pull-down.
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
The internal Pull-down is disabled after PCH_PWROK de-asserts.



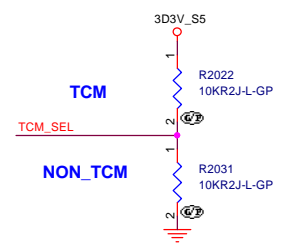
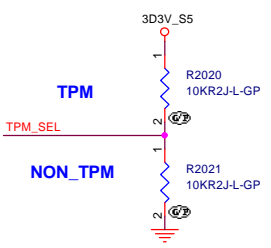
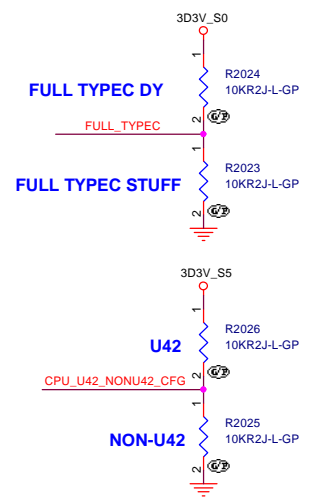
0913 SVT EC041



0913 SVT EC041



20170405_need check again

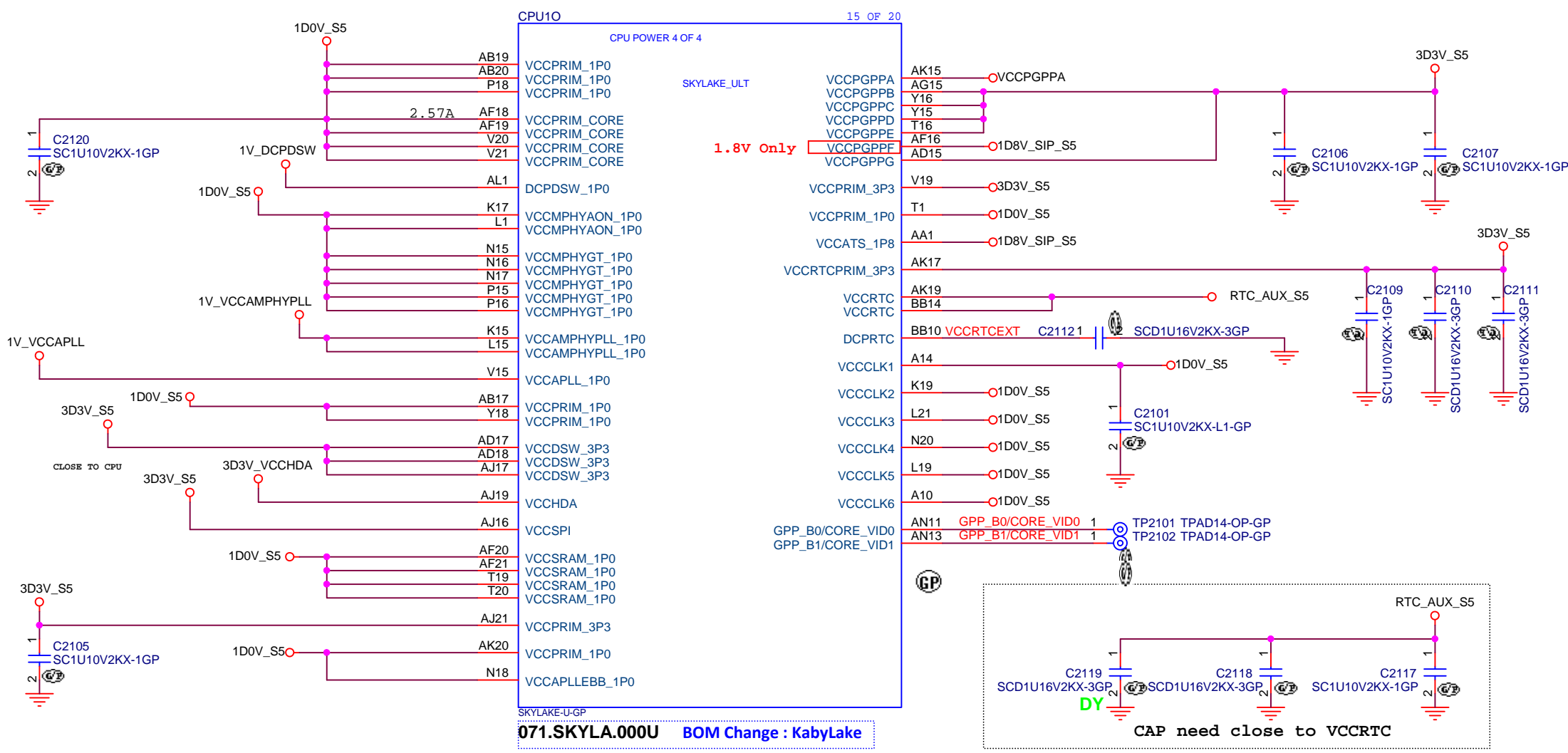


<Variant Name>

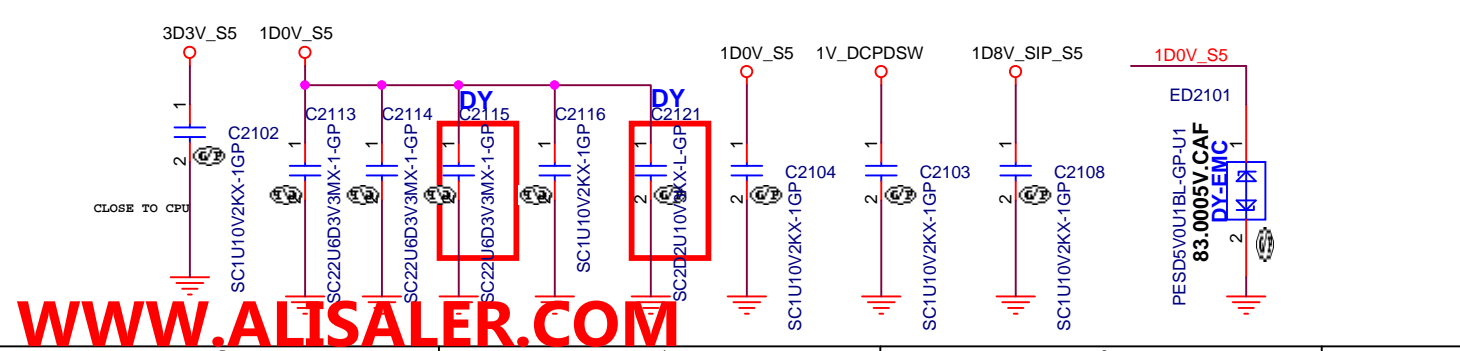
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title CPU (LPSS/UART/ISH)
Size A3 Document Number Unicorn LV530 KBL MB18A Rev
Date: Friday, December 15, 2017 Sheet 20 of 105

Main Func = PCH



071.SKYLA.000U BOM Change : Kabylake



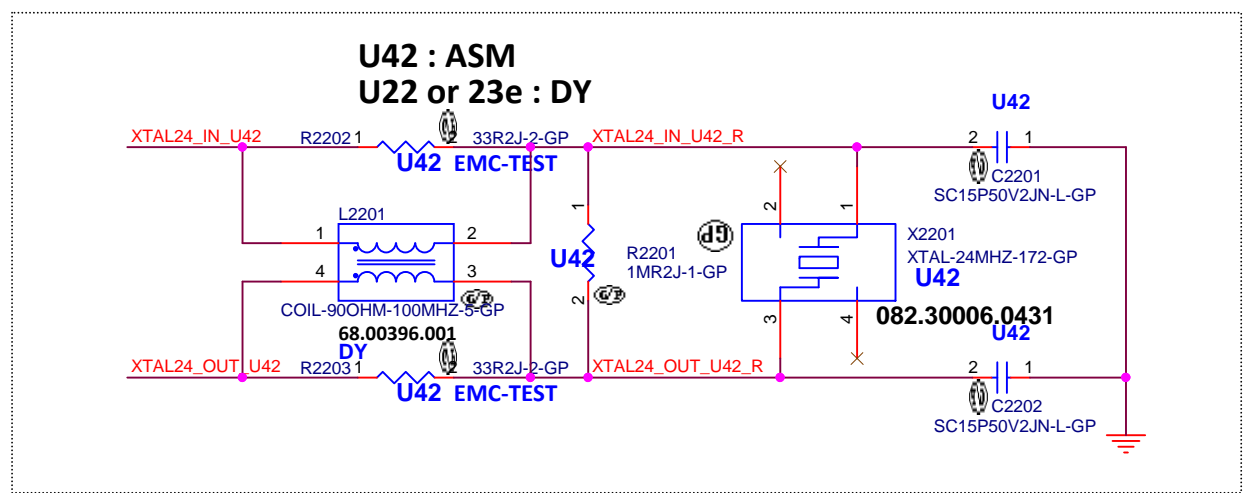
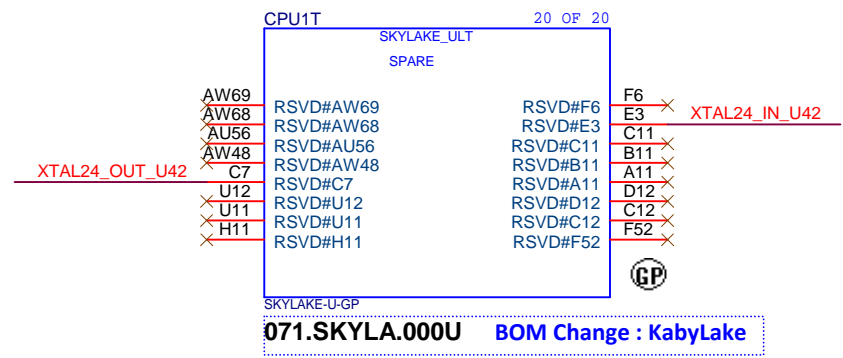
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (POWER1)**

Size A4 Document Number: **Unicorn LV530 KBL MB GA** Rev

Date: Friday, December 15, 2017 Sheet 21 of 105



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **CPU (RSVD)**

Size A4 Document Number **Unicorn LV530 KBL MB GA** Rev

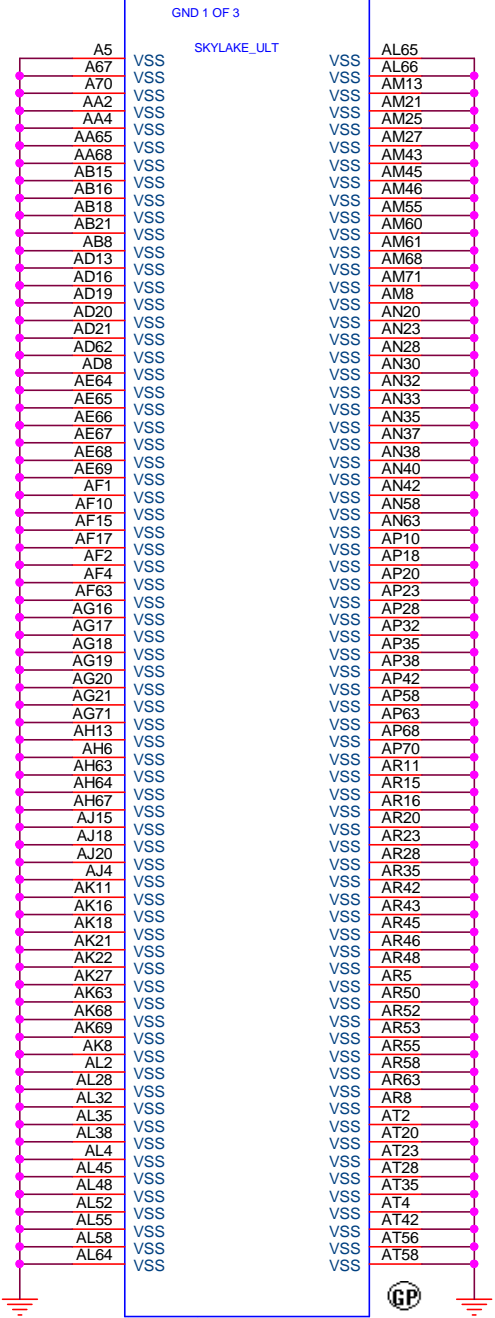
Date: Friday, December 15, 2017 Sheet 22 of 105

Main Func = PCH

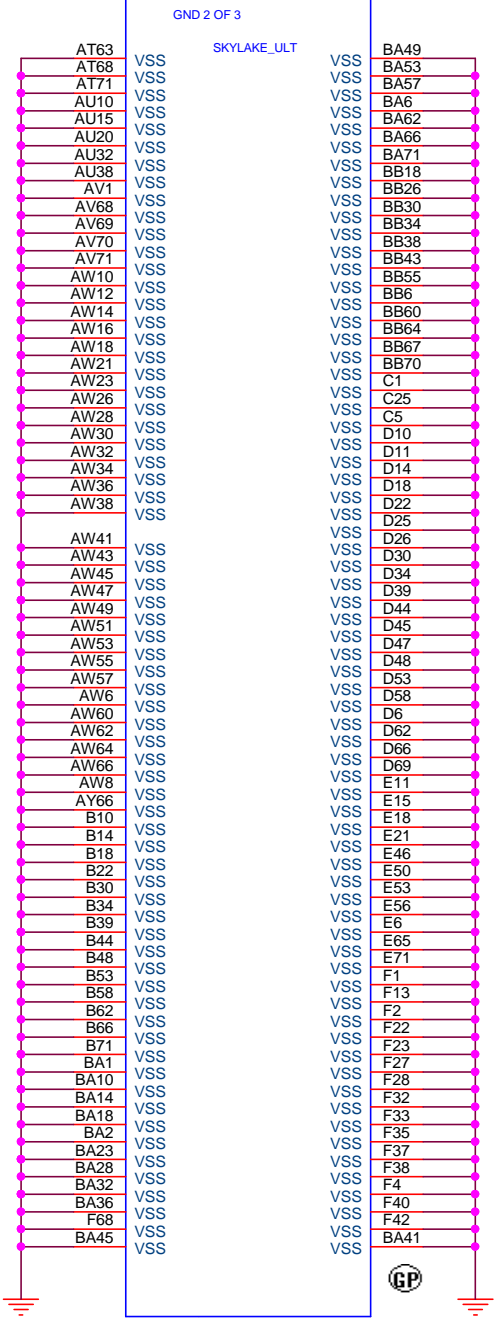
CPU1P 16 OF 20

CPU1Q 17 OF 20

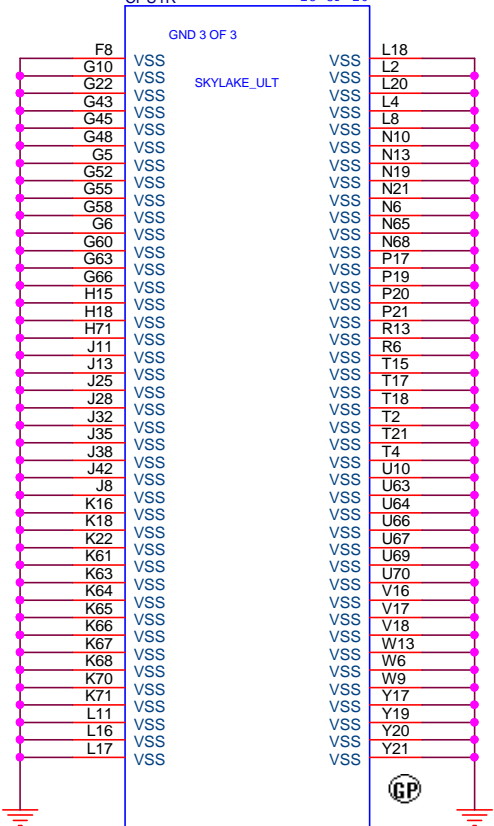
CPU1R 18 OF 20



SKYLAKE-U-GP
071.SKYLA.000U BOM Change : KabyLake



SKYLAKE-U-GP
071.SKYLA.000U BOM Change : KabyLake

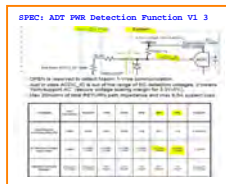
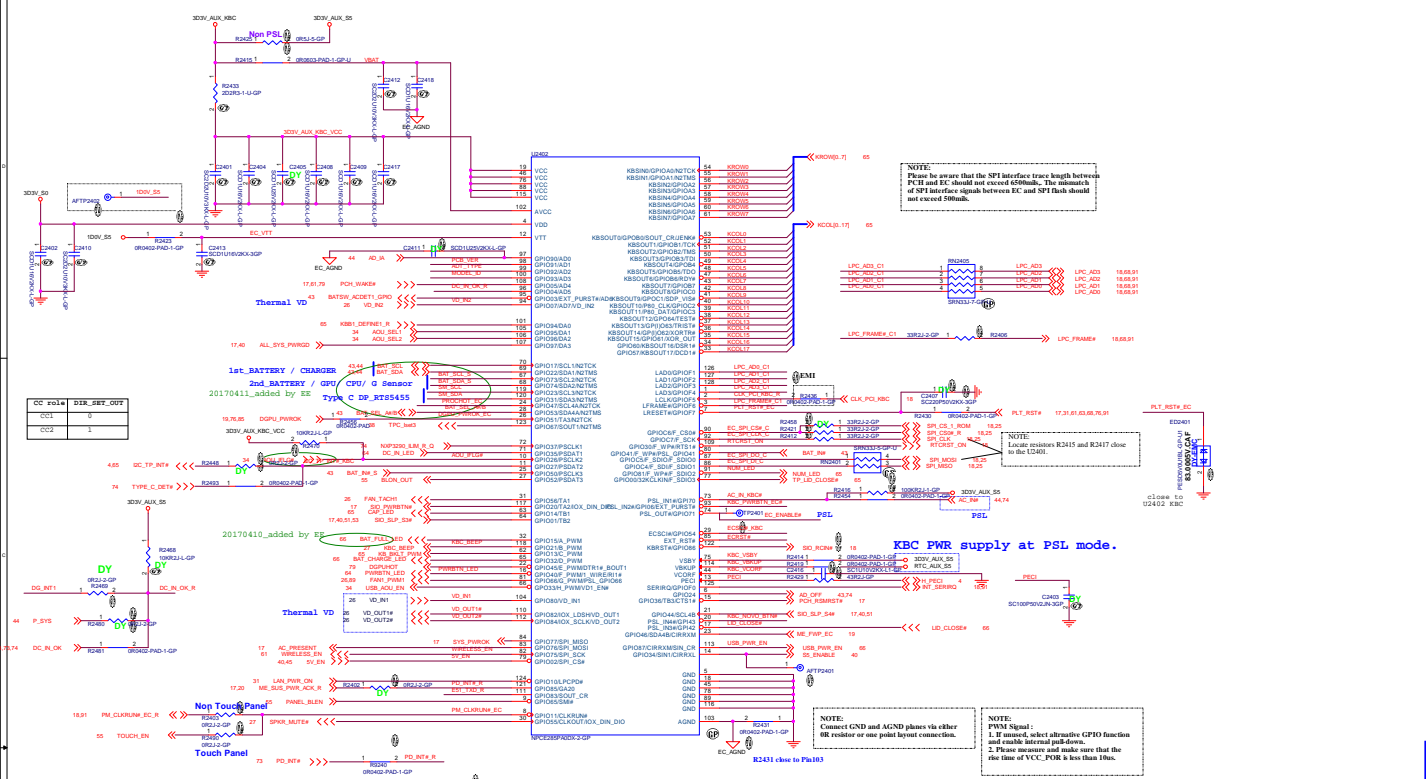


SKYLAKE-U-GP
071.SKYLA.000U BOM Change : KabyLake

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title CPU (VSS)		
Size Custom	Document Number	Rev
Unicorn LV530 KBL MB 6A		
Date: Friday, December 15, 2017	Sheet 23 of 105	

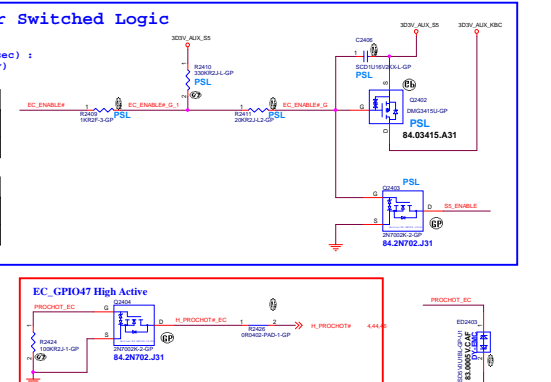
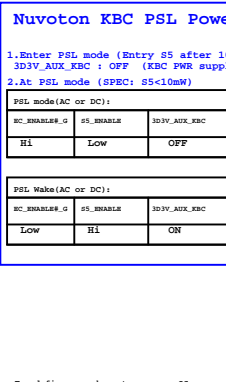
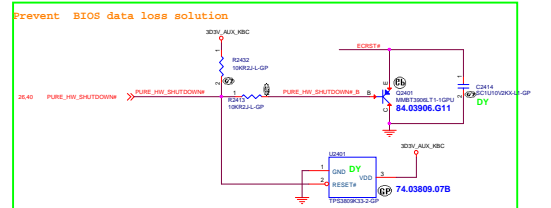
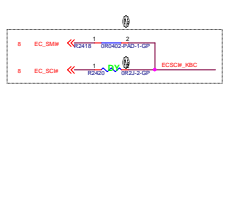
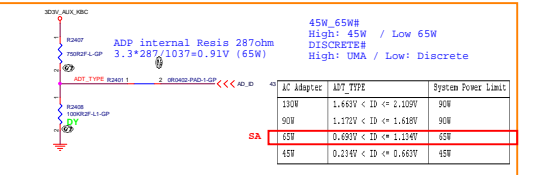
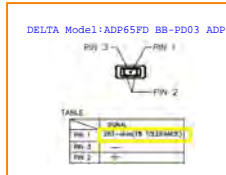


PCB VERSION

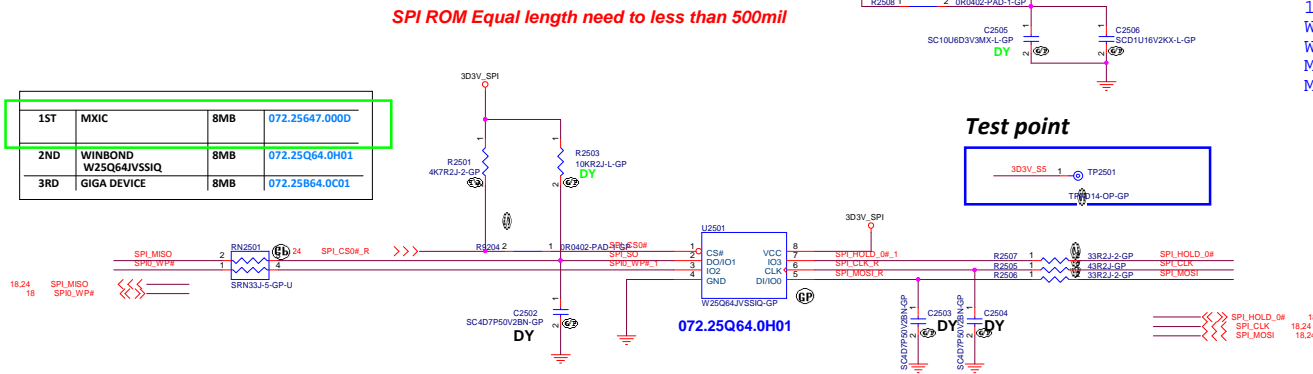
PCB VERSION	ADP(PWR)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
0A	100.0K	100.0K	64.10025.10K	3.0V
E53_KBL	100.0K	20.0K	64.20025.10K	2.75V
V30_KBL	100.0K	33.0K	64.33025.10K	2.8V
V30_KBL	100.0K	47.0K	64.47025.10K	2.34V
NA	100.0K	64.9K	64.64925.10K	2.8V
V10-15K8	V10 EC001	100.0K	64.76825.10K	1.87V
NA	100.0K	215.0K	64.21535.10K	1.04V

PCB VERSION

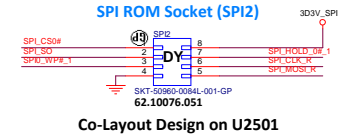
PCB VERSION	ADP(PWR)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
0B	100.0K	20.0K	64.20025.10K	2.75V
0C	100.0K	33.0K	64.33025.10K	2.8V
0D	100.0K	47.0K	64.47025.10K	2.34V
-1	100.0K	64.9K	64.64925.10K	2.8V
-1M	100.0K	76.8K	NA	1.87V
PVT BC051	-2	NA	NA	NA
-3	100.0K	100.0K	100.0K	1.64V
-4	100.0K	133.0K/133.5K/134.0K	1.71V	1.41V
-4	100.0K	174.0K/174.47K/174.94K	1.20V	1.20V



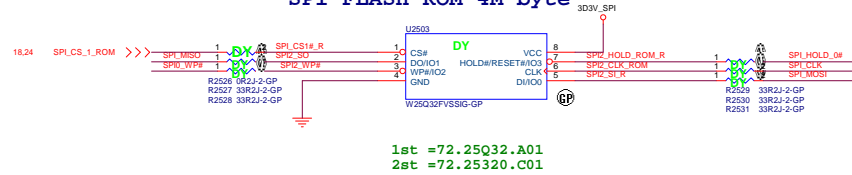
SSID = Flash.ROM



- 16MB SOIC8
 WINBOND W25Q128FVSIQ/ 72.25128.0E1
 WINBOND W25Q128FVSIQ/ 072.25128.0A1
 MACRONIX MX25L12873FM2I-10G/ 72.12873.001
 MACRONIX MX25L12873FM2I-10G/ 072.25128.0B11

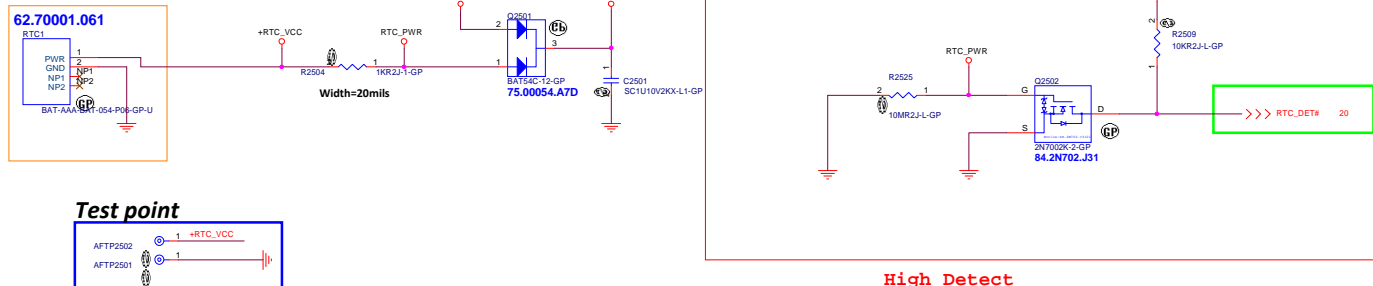


SPI FLASH ROM 4M byte



SSID = RBATT

20170320_need check pin define with ME



High Detect
Need to Check whether to PD in PCH Side

<Variant Name>

緯創資通 Wistron Corporation
 21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsichang, Taipei Hsien 221, Taiwan, R.O.C.

SPI/RTC

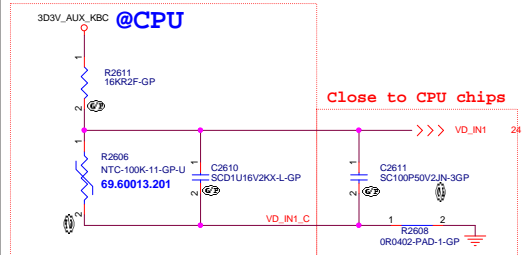
File: **Unicorn LV530_KBL_MB**

Size: A2 Document Number: Rev. 1.06

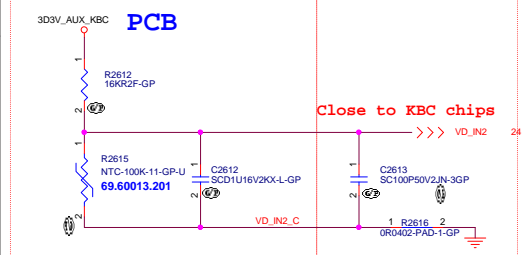
Date: Friday, December 15, 2017 Sheet: 26 of 106

Main Func = Thermal Sensor

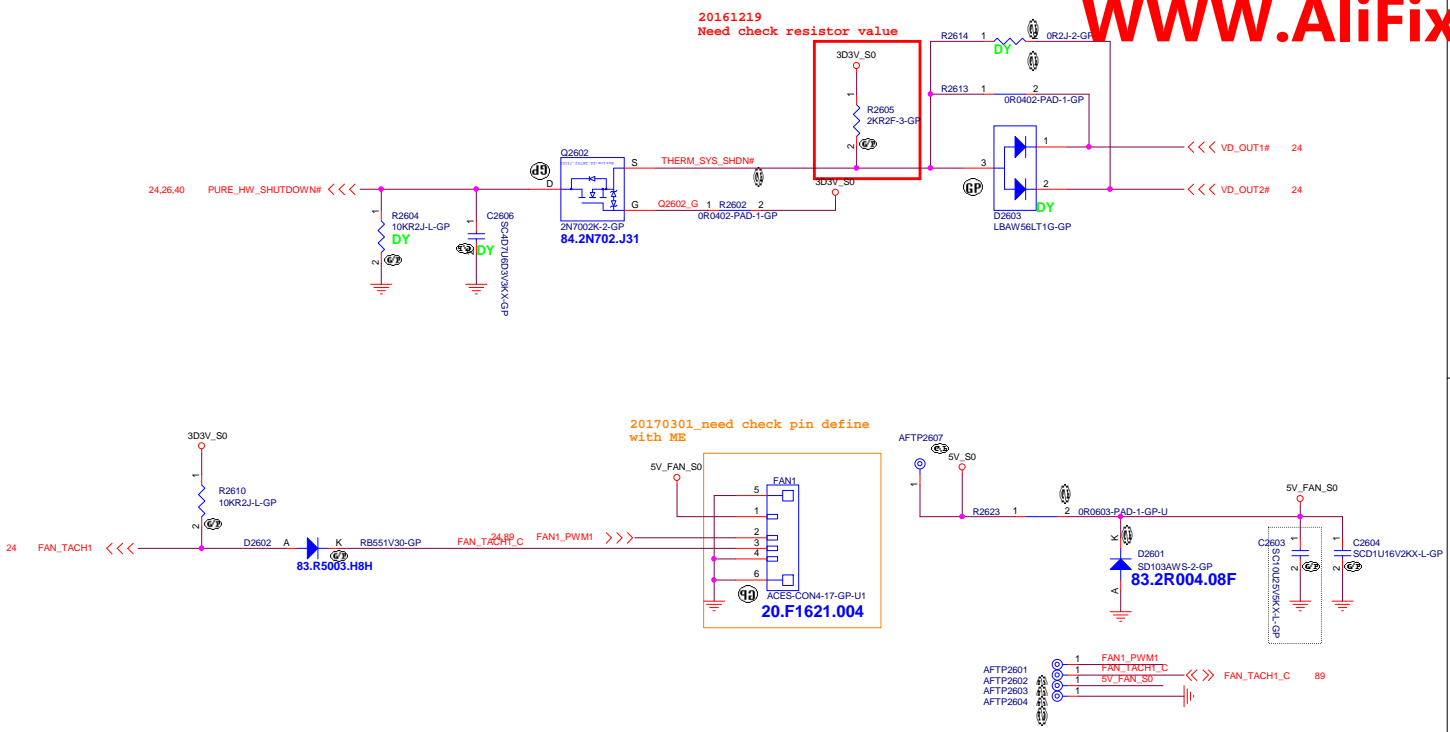
Close to Thermal sensor



Close to CPU chips

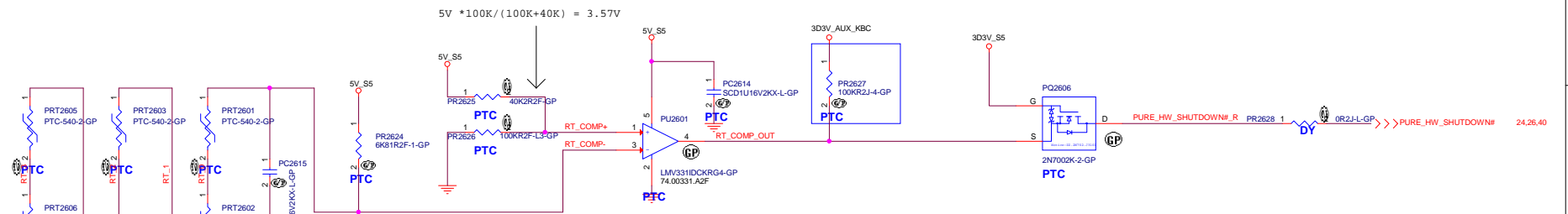


Close to KBC chips



PURE_HW_SHUTDOWN# logic table

signal name	Sys. Temp < Ref. Temp	Sys. Temp > Ref. Temp
RT_COMP_OUT	High	Low
PURE_HW_SHUTDOWN#	High	Low



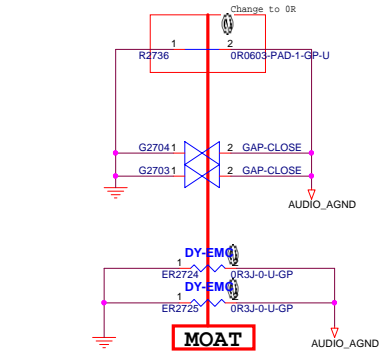
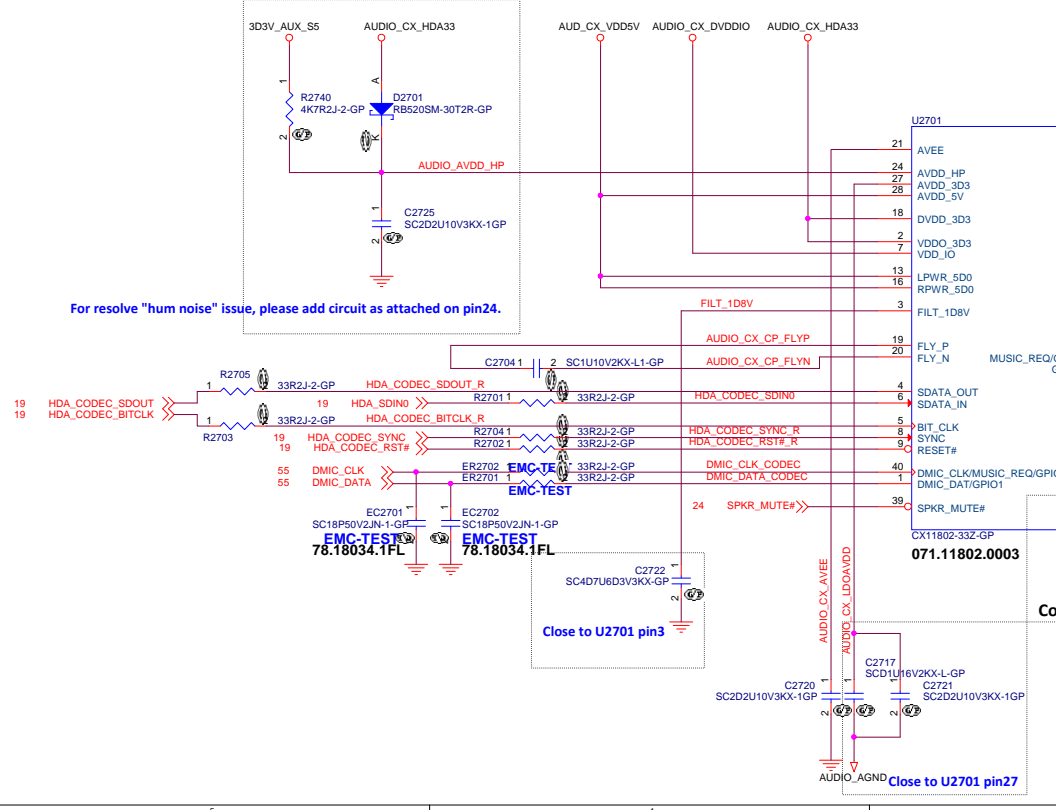
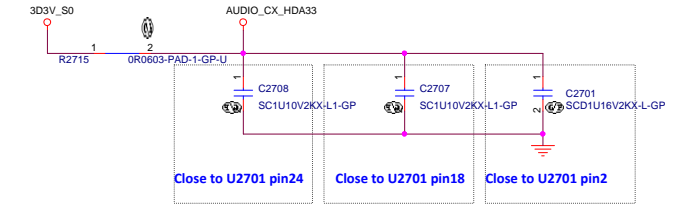
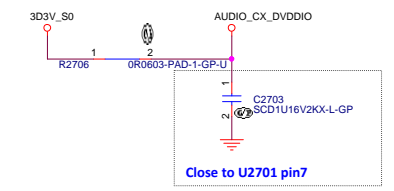
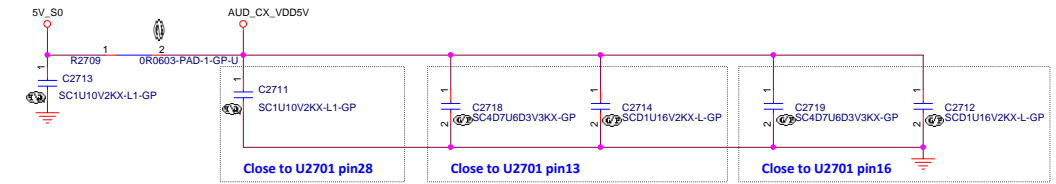
OBS REASON: Cost of 74.00331.C2F is not competitive. Pls use BCD 74.00331.I2F and TI 74.00331.A2F for instead.

<Variant Name>

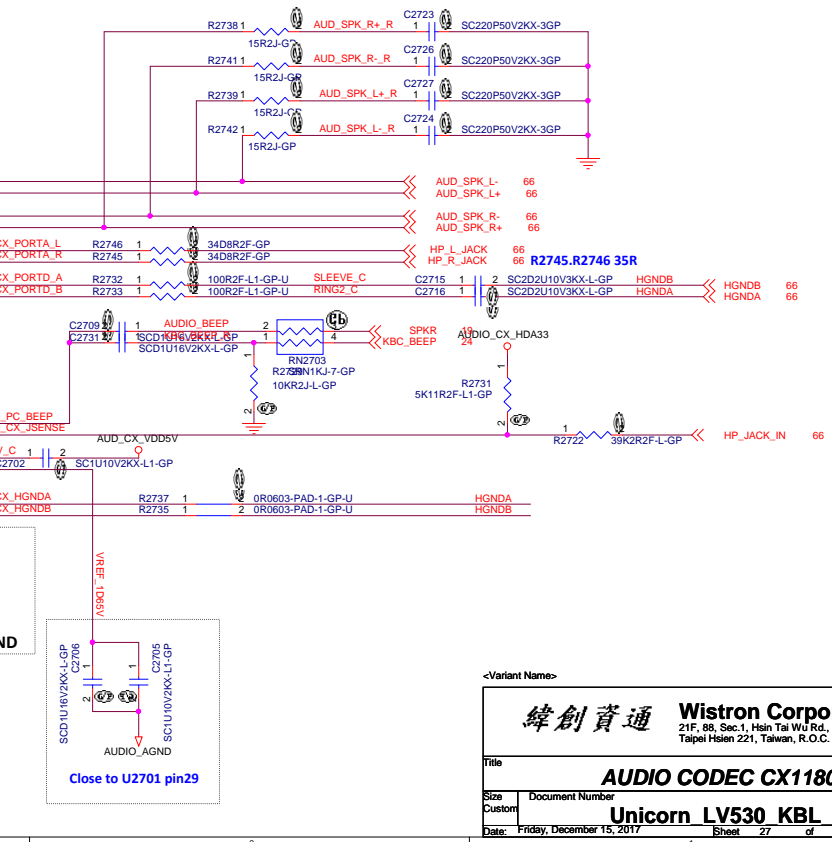
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hei Tai Wu Rd., Hsichih, Taipei Heien 221, Taiwan, R.O.C.

Title: **THERMAL/FAN**

Size: Document Number
 Custom: Unicorn LV530 KBL ME19A
 Date: Friday, December 15, 2017 Sheet 26 of 105



Install snubber networks on each net of SPKs helps control the overshoot/undershoot at the class-D outputs.



<p>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>	
<p>AUDIO CODEC CX11802</p>	
<p>Spec Custom</p>	<p>Document Number Unicorn LV530 KBL MB19A</p>
<p>Date: Friday, December 15, 2017</p>	<p>Rev Sheet 27 of 105</p>

TABLE : Automatic Switching Mode (CFG0 = H)

SW (DDI_PRIORITY2)
L Port 1 has higher priority when both ports are plugged
H Port 2 has higher priority when both ports are plugged

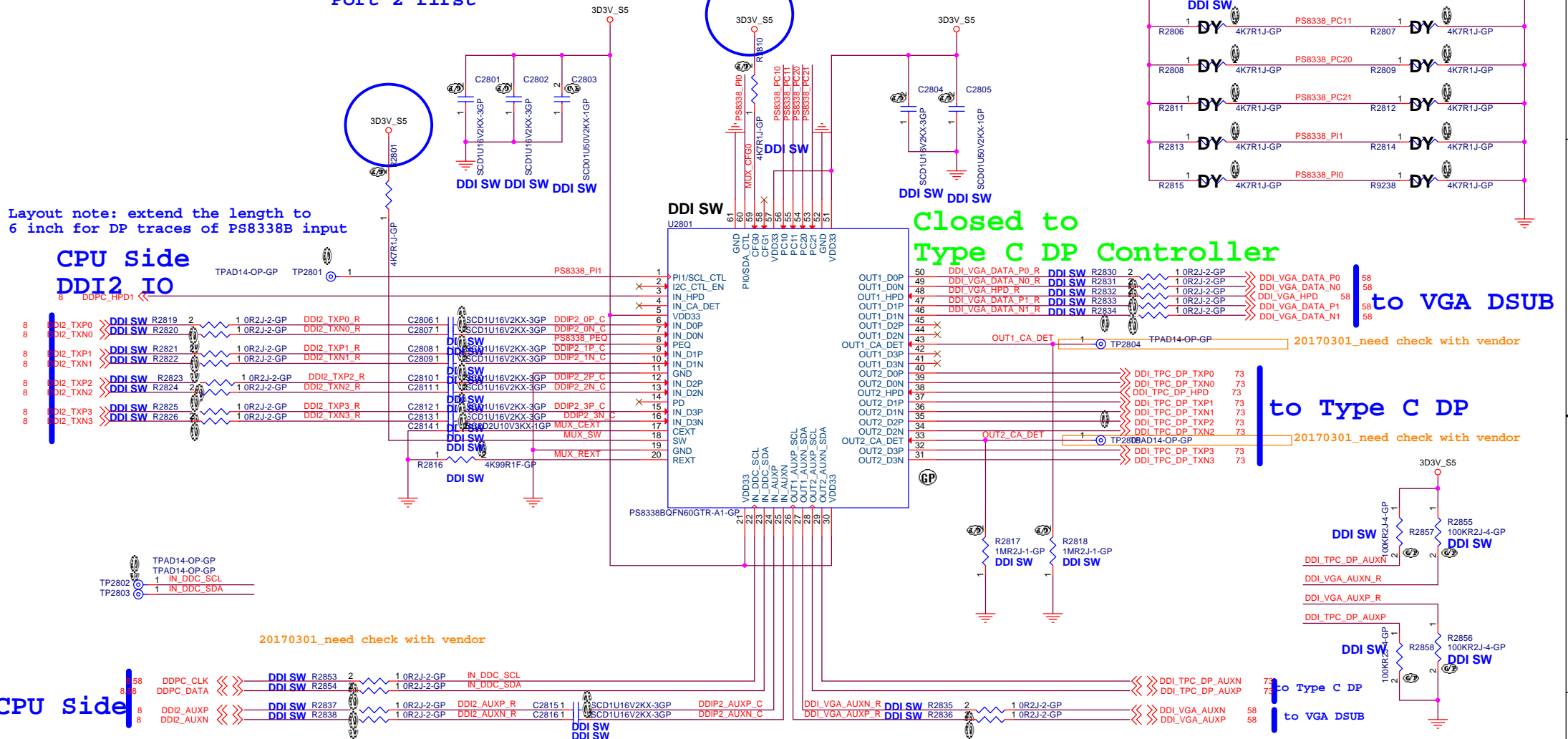
For Automatic Switching Mode (CFG0 = H):

SW = L: Port1 has higher priority when both ports are plugged (default)

SW = H: Port2 has higher priority when both ports are plugged

Overwritten by I2C register in I2C Control Mode

Port 2 first



Bypass DDI SW

DDI2_TXP0	VGA	R2839	2	1 0R2J-2-GP	DDI2_TXP0 BYPASS	VGA	R2840	2	1 0R2J-2-GP	DDI_VGA_DATA_P0
DDI2_TXN0	VGA	R2841	2	1 0R2J-2-GP	DDI2_TXN0 BYPASS	VGA	R2842	2	1 0R2J-2-GP	DDI_VGA_DATA_N0
DDI2_TXP1	VGA	R2843	2	1 0R2J-2-GP	DDI2_TXP1 BYPASS	VGA	R2844	2	1 0R2J-2-GP	DDI_VGA_DATA_P1
DDI2_TXN1	VGA	R2845	2	1 0R2J-2-GP	DDI2_TXN1 BYPASS	VGA	R2846	2	1 0R2J-2-GP	DDI_VGA_DATA_N1
DDI2_AUXN	VGA	R2847	2	1 0R2J-2-GP	DDI2_AUXN BYPASS	VGA	R2848	2	1 0R2J-2-GP	DDI_VGA_AUXN
DDI2_AUXP	VGA	R2849	2	1 0R2J-2-GP	DDI2_AUXP BYPASS	VGA	R2850	2	1 0R2J-2-GP	DDI_VGA_AUXP
DDPC_HPD1	VGA	R2851	2	1 0R2J-2-GP	DDPC_HPD1 BYPASS	VGA	R2852	2	1 0R2J-2-GP	DDI_VGA_HPD

Wistron Corporation

21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

DDI Switch

Unicorn LV530 KBL MB13A

Rev 1.0

Date: Friday, December 15, 2017

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**INTERNAL STEREO SPEAKERS
MOVE TO SMALL BOARD**

<Variant Name>		
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title AUDIO SPEAKER		
Size A3	Document Number Unicorn LV530 KBL MB13A	Rev 1
Date: Friday, December 15, 2017	Sheet 29	of 105

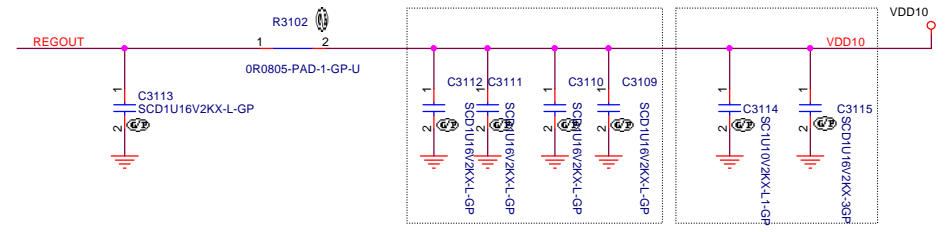
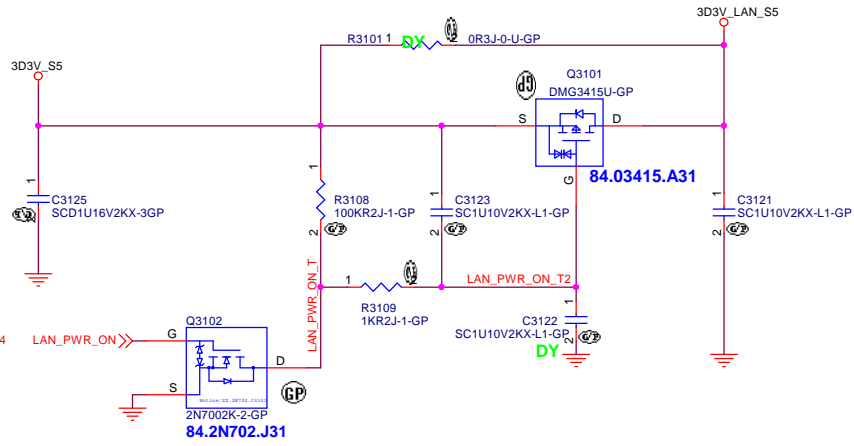
<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
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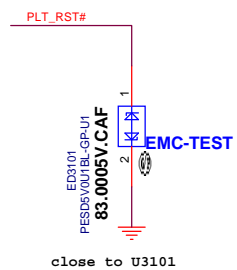
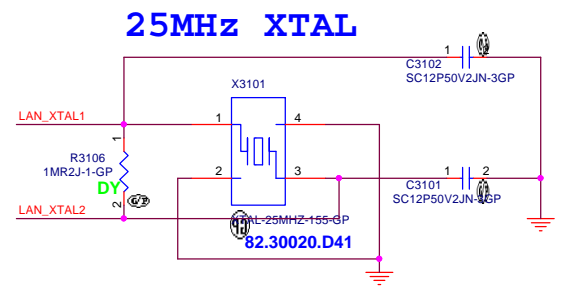
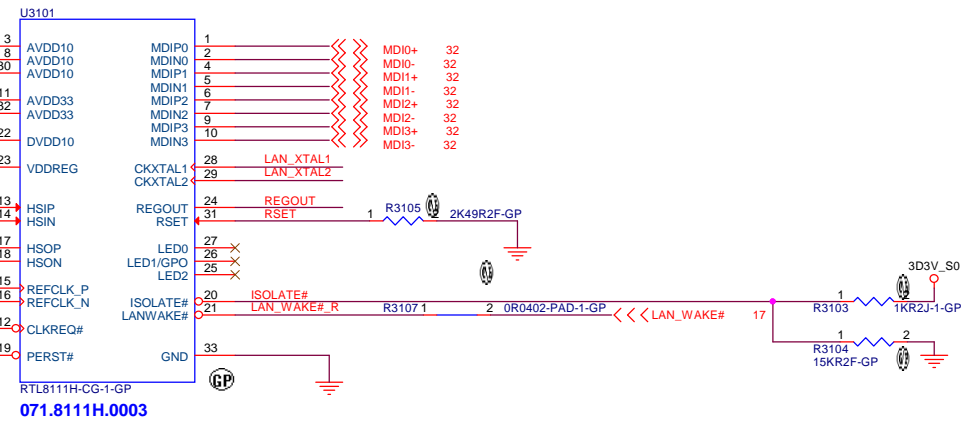
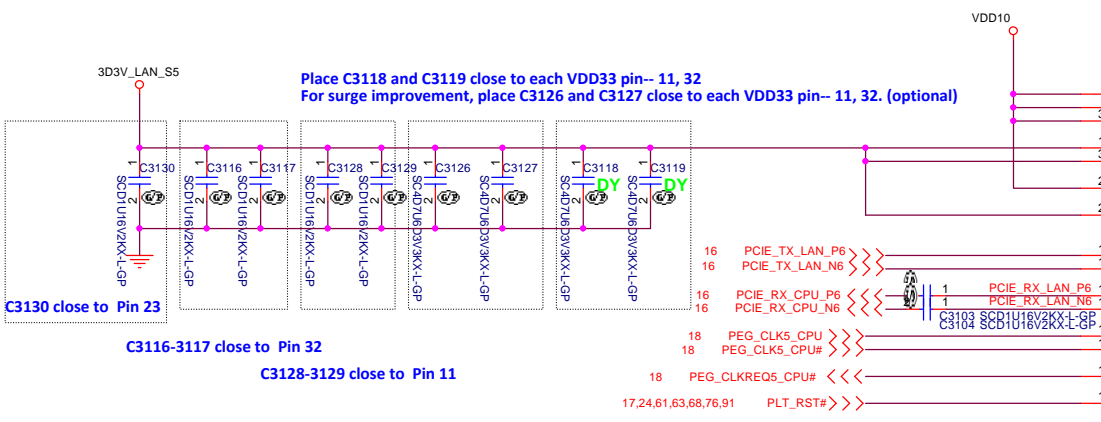
(RESERVED)

Size	Document Number	Rev
A4	Unicorn_LV530_KBL_MB14BOHOL	SA

Date:	Sheet	of	105
Friday, December 15, 2017	30	1	105



For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
 *Place C3109 to C3112 close to each VDD10 pin-- 3, 8, 22, 30
 For RTL8111G(S)/ RTL8111GUS/ RTL8106EUS
 *Place C3114 and C3115 close to each VDD10 pin-- 22 (Reserved)



<Variant Name>

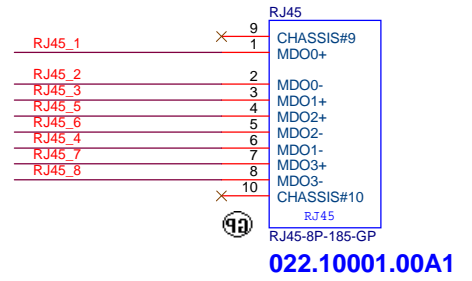
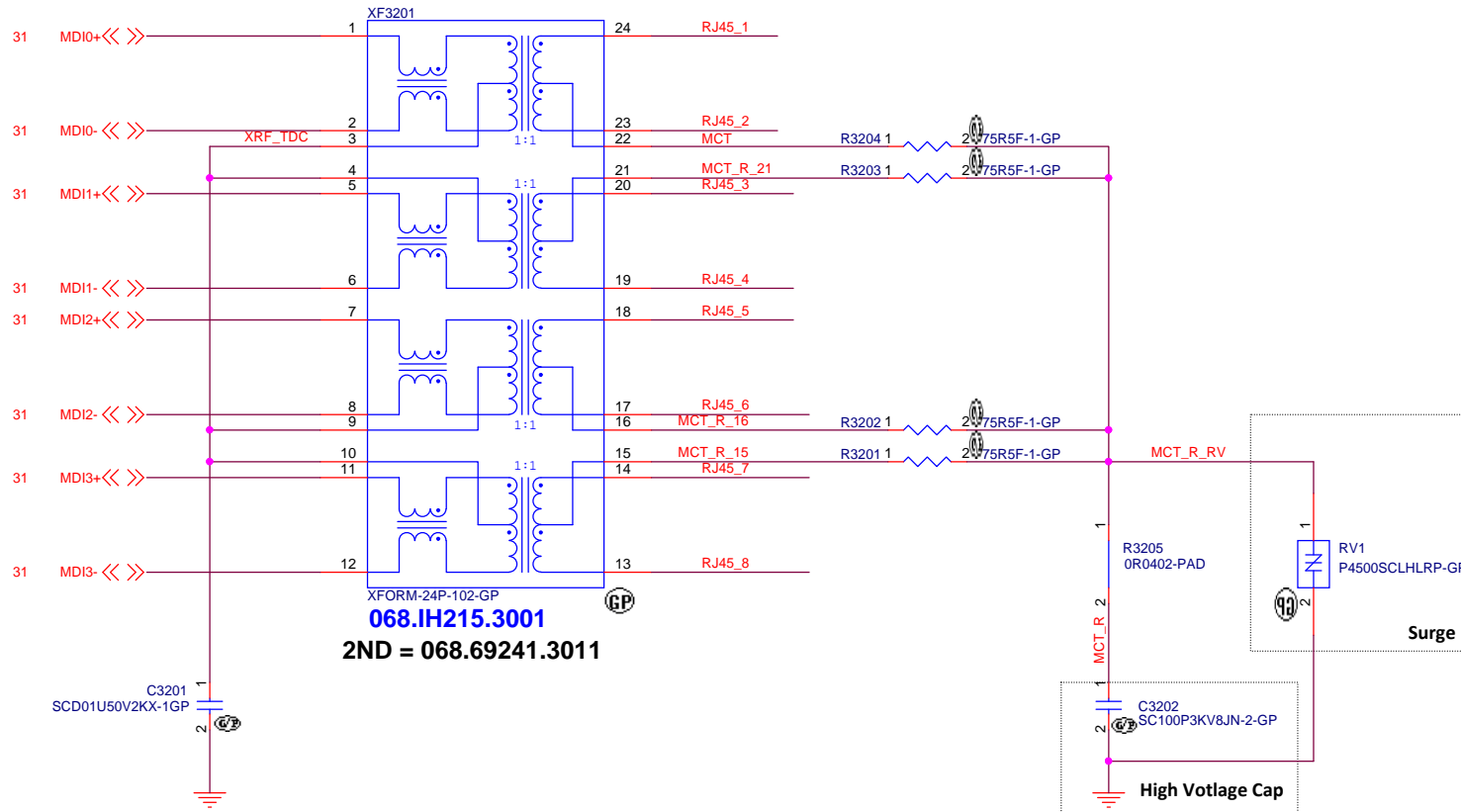
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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Title: **LAN RTL8111H**

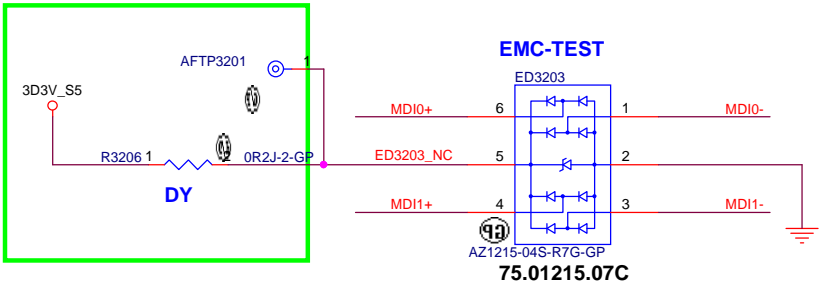
Size A3 Document Number: **V530 Unicorn LV530 KBISAMB1** Rev

Date: Friday, December 15, 2017 Sheet 31 of 105

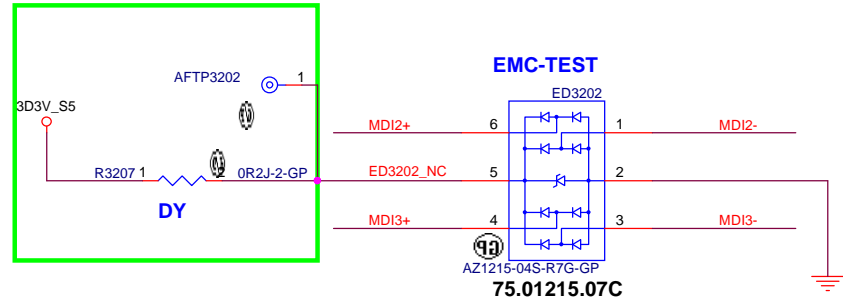
10/100M/1000M Lan Transformer



20170606
EMC Tim Lee requirement



20170606
EMC Tim Lee requirement



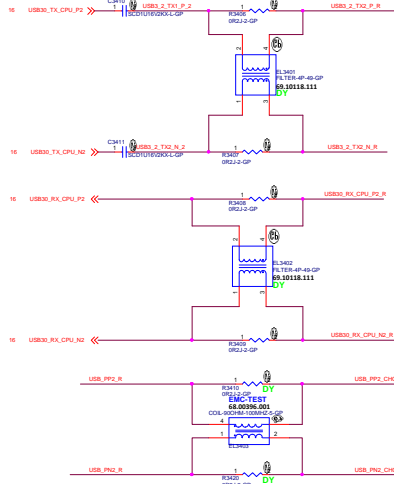
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
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RJ45			
Size	Document Number	Rev	
Custom	Unicorn LV530 KBL MB13A		
Date:	Friday, December 15, 2017	Sheet	32 of 105

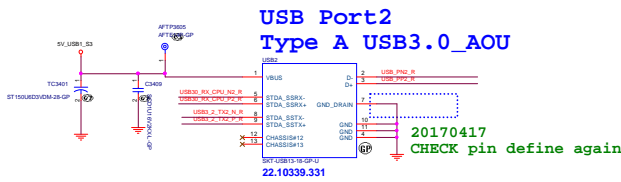
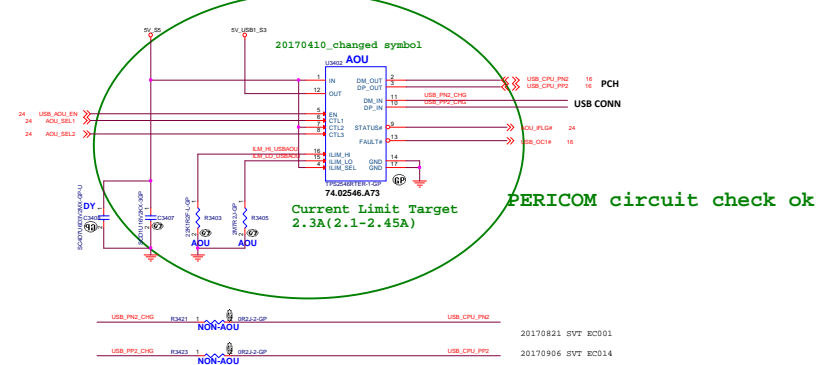
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title (RESERVED)		
Size A3	Document Number Unicorn_LV530_KBL_MB14V530	Rev SA
Date: Friday, December 15, 2017	Sheet 33	of 105

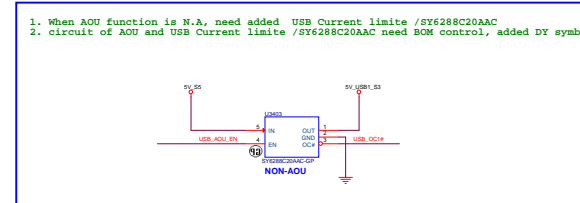
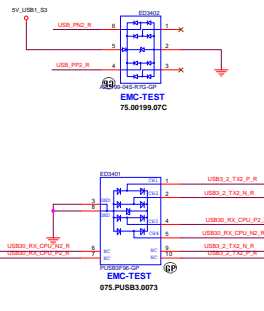
needReserve USB2.0 by pas AOU



AOU
1ST,
TI, 74.02546.A73
IC PWR SW TPS2546RTER QFN 16P(REV 1.1)
2ND
PERICOM, 074.52546.0A73
IC PWR SW PI5USB2546ZHEX TQFN 16P REV.X



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	St-dA_SSRX-	SuperSpeed RX
6	St-dA_SSRX+	
7	GND	
8	St-dA_SSTX-	SuperSpeed TX
9	St-dA_SSTX+	



- When AOU function is N.A., need added USB Current limits /SY6288C20AAC
- circuit of AOU and USB Current limits /SY6288C20AAC need BOM control, added by symbol

RESERVED

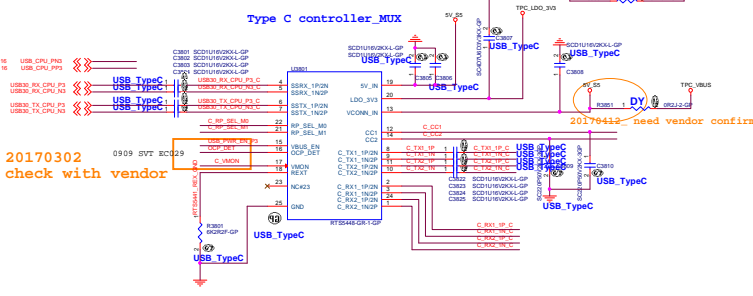
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Date: Friday, December 15, 2017	Sheet 35 of 105

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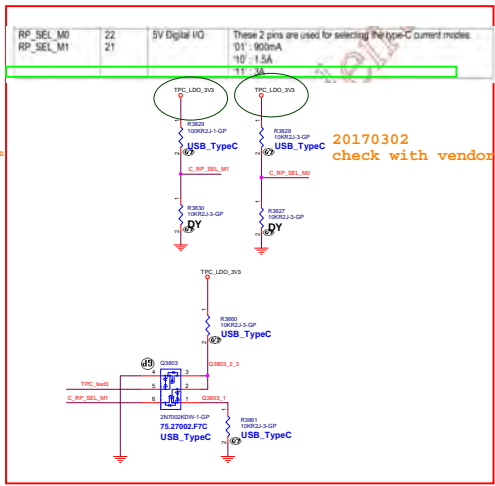
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		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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File	Size	Document Number	Rev
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Date: Friday, December 15, 2017	Sheet	96	of 105

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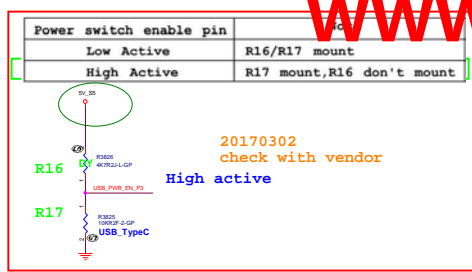
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Size A4	Document Number Unicorn LV530 KBL MB SA		Rev 1A
Date: Friday, December 15, 2017		Sheet 37	of 105



20170302 check with vendor

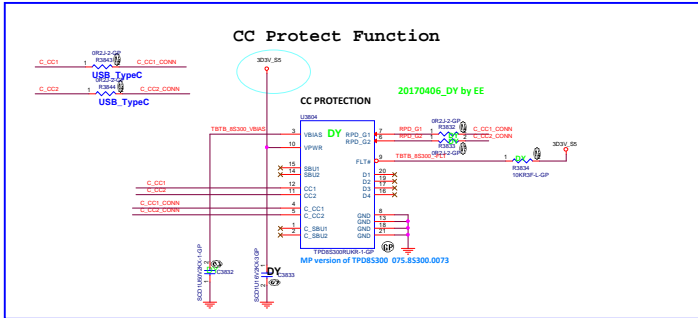
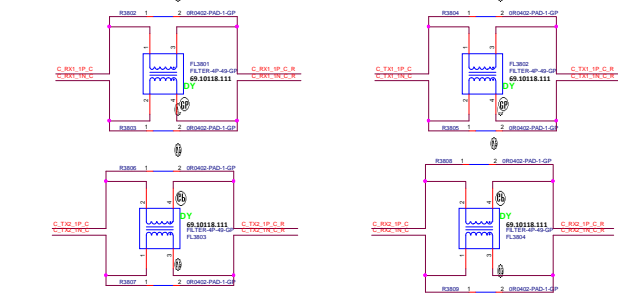


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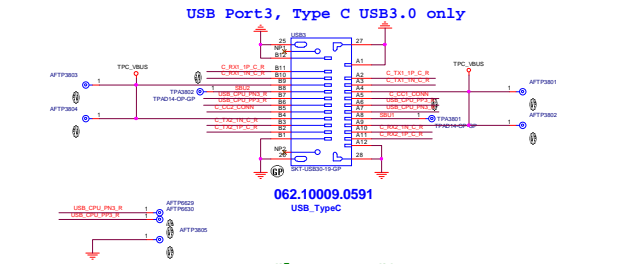
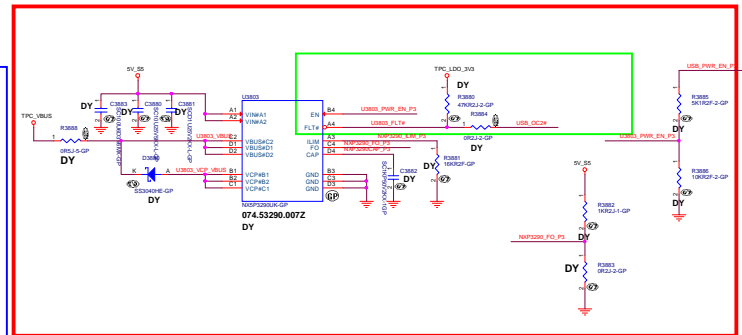


20170302 check with vendor

Power switch enable pin	Note
Low Active	R3826/R3825 mount
High Active	R3825 mount, R3826 don't mount

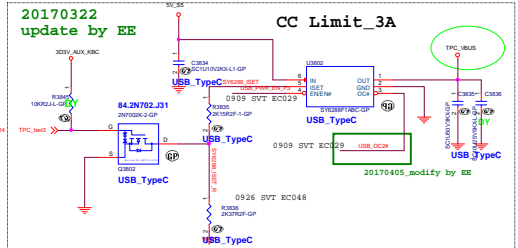


20170406.DY by EE



062.10009.0591 USB_TypeC

Close to CONN



20170322 update by EE

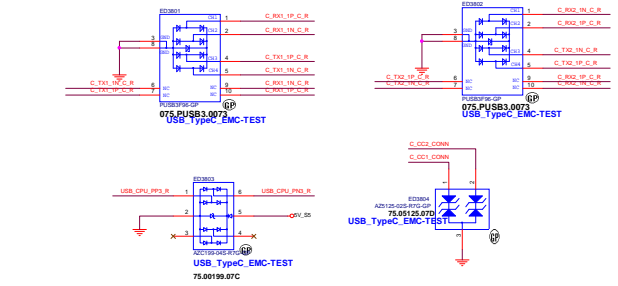
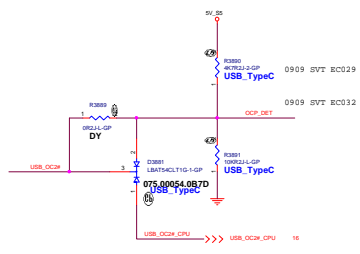
- 1. AC: 15W / 3A, 系統功耗不足降至4.5W / 0.9A
- 2. DC: 4.5W / 0.9A

Over-current protection
The SY6288F1/F2 supports Current limit programming. Connect a resistor R_{SET} from ISET pin to ground to program the current limit:

$$I_{LIM} (A) = 6800 / R_{SET} (\Omega)$$

The minimum current limit is 0.4A. Current limit beyond 4A is not recommended.

- R3835 / 2.15K >> 3.16A
- R3835 / 2.15K + R3836 / 5.1K >> 0.94A



<Variant Name>

<Title>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

A

Document Number

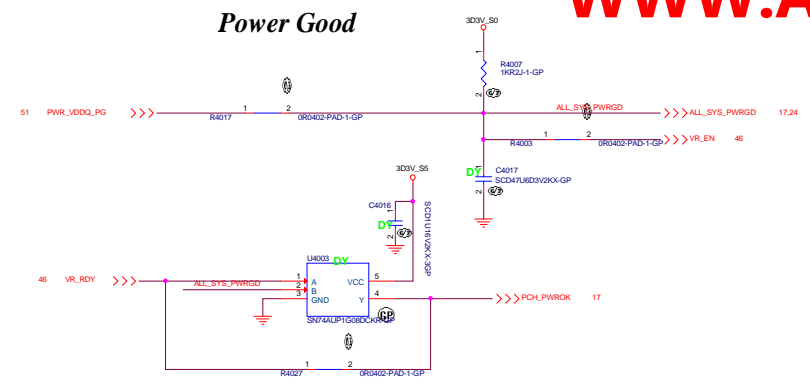
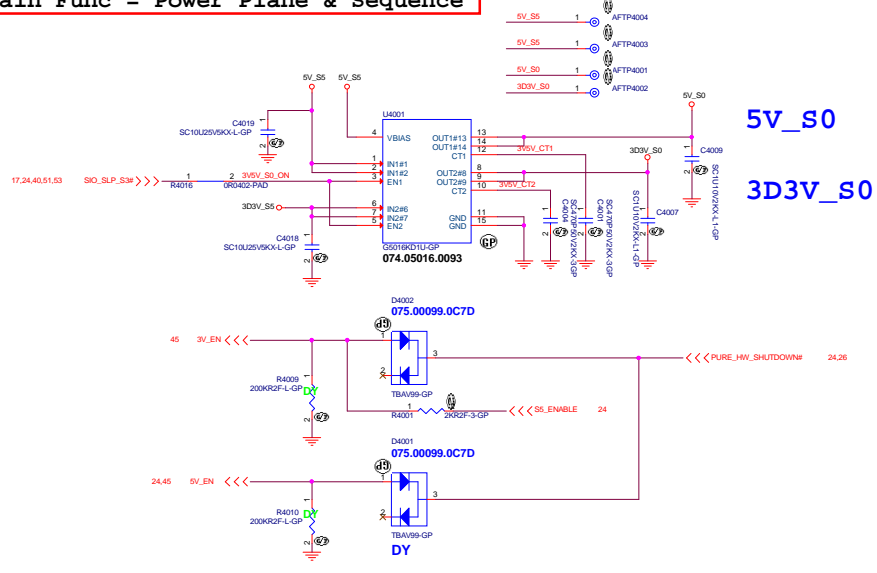
Unicorn_LV530_KBL_MB14BOH01SA

Rev

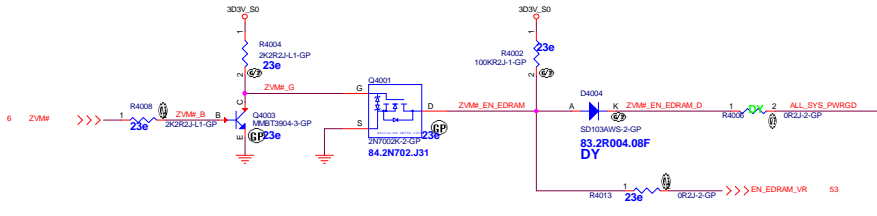
Date: Friday, December 15, 2017

Sheet 39 of 105

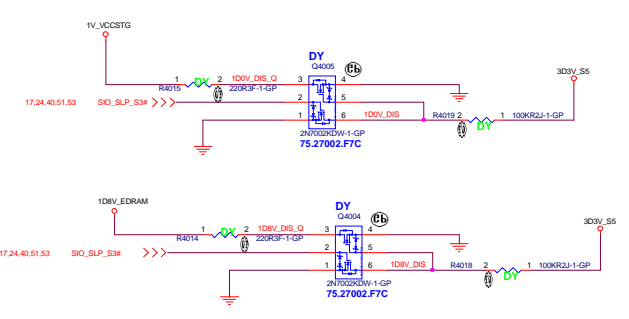
Main Func = Power Plane & Sequence



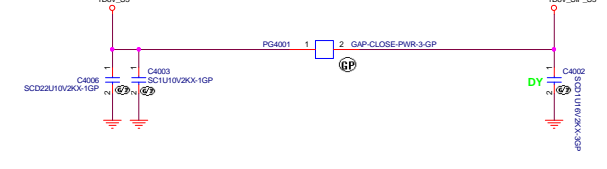
GT3 Low Power Circuit (ZVM)



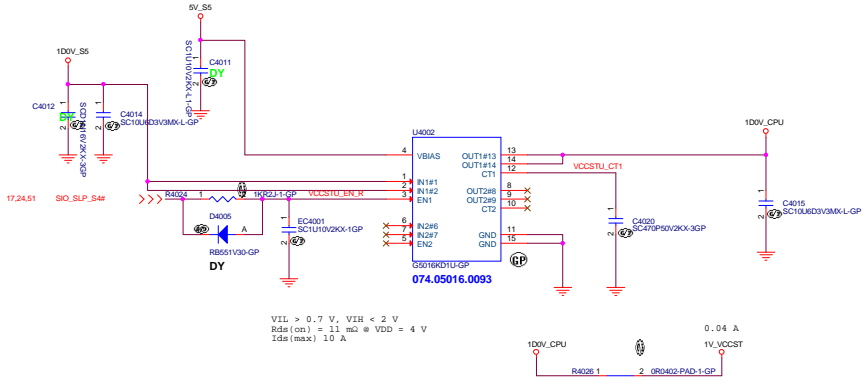
Discharge circuit



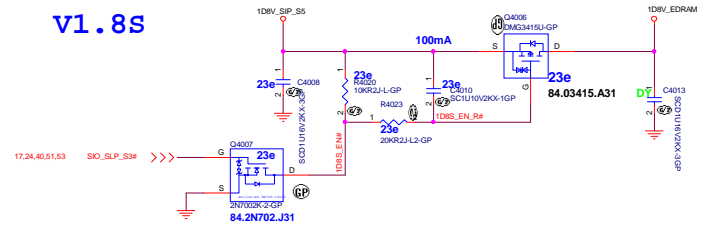
V1.8A



VCCSTU



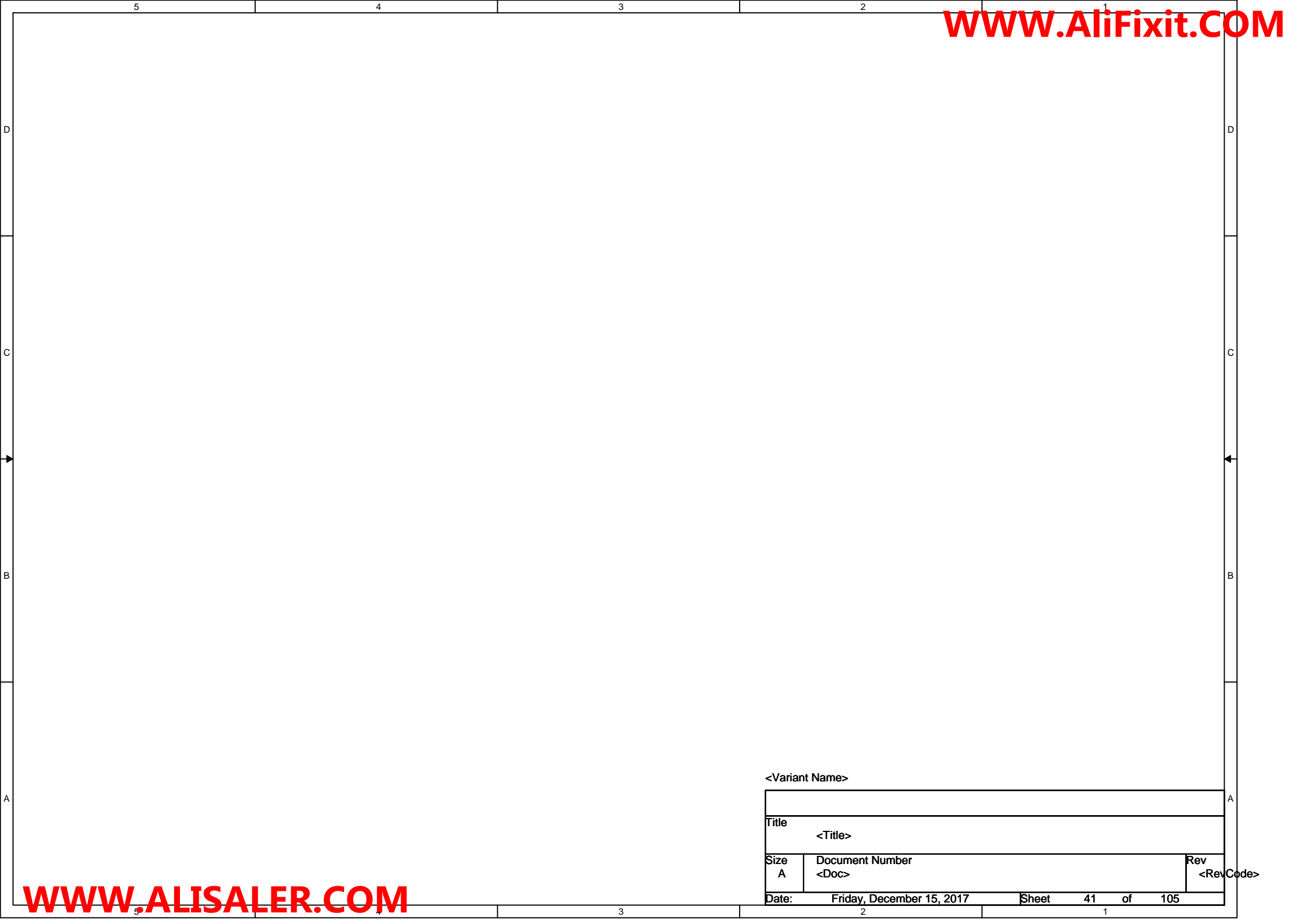
V1.8S



561280 KBL DY PDG Rev2.0 Notes:
On power up sequence, VCC0PC_ip8 must never ramp up after VCC0PC/VCC0PIO under any circumstance.
There are no ramp down requirements between VCC0PC_ip8 and VCC0PC/VCC0PIO.
Platform must guarantee VCC0PC/VCC0PIO falls do not start ramping back up for any reason while VCC0PC_ip8 is ramping down or off.

V1L > 0.7 V, VIN < 2 V
Rds(on) = 11 mΩ @ VDD = 4 V
Ids(max) 10 A

-Variant Name-	
緯創資通	
Wistron Corporation	
2/F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.	
File	POWER PLAN EN&SEQUENCE
Scale	Document Number
Customer	Unicorn LV530 KBL MBI
Date: Friday, December 16, 2011	Rev: 040HOL
Sheet: 40	of 106



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Size	Document Number	Rev
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Date:	Friday, December 15, 2017	Sheet	41	of	105
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size
A4

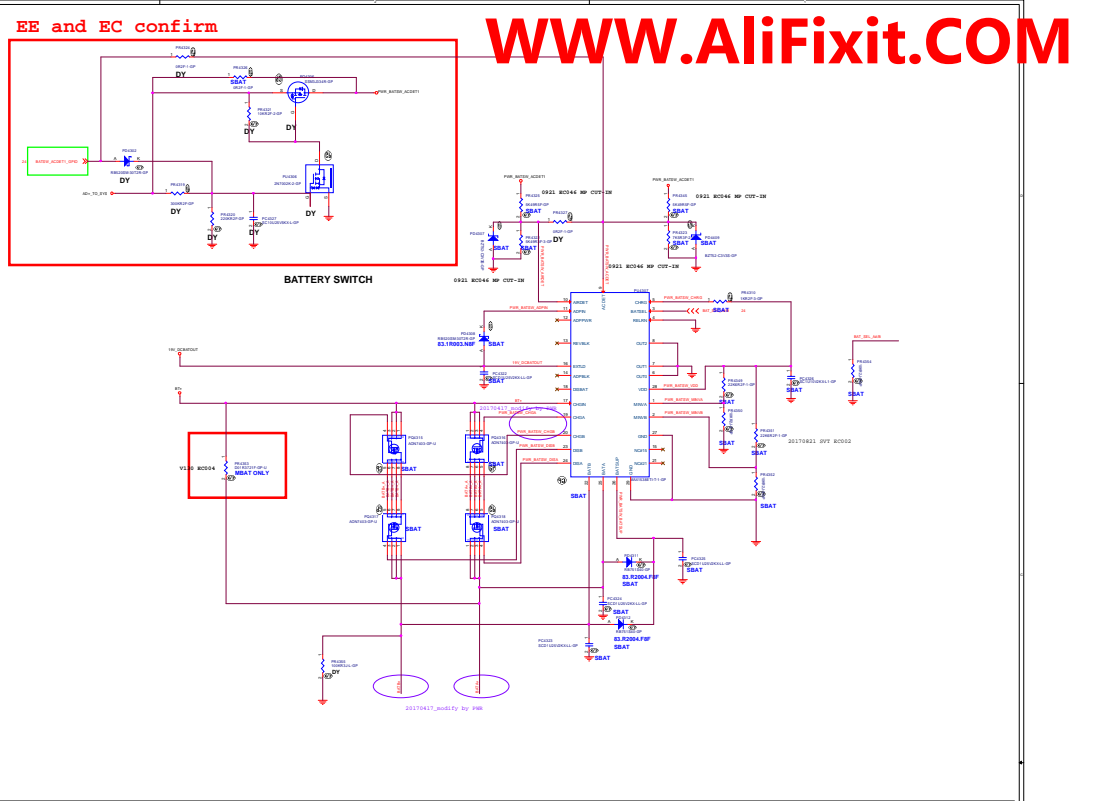
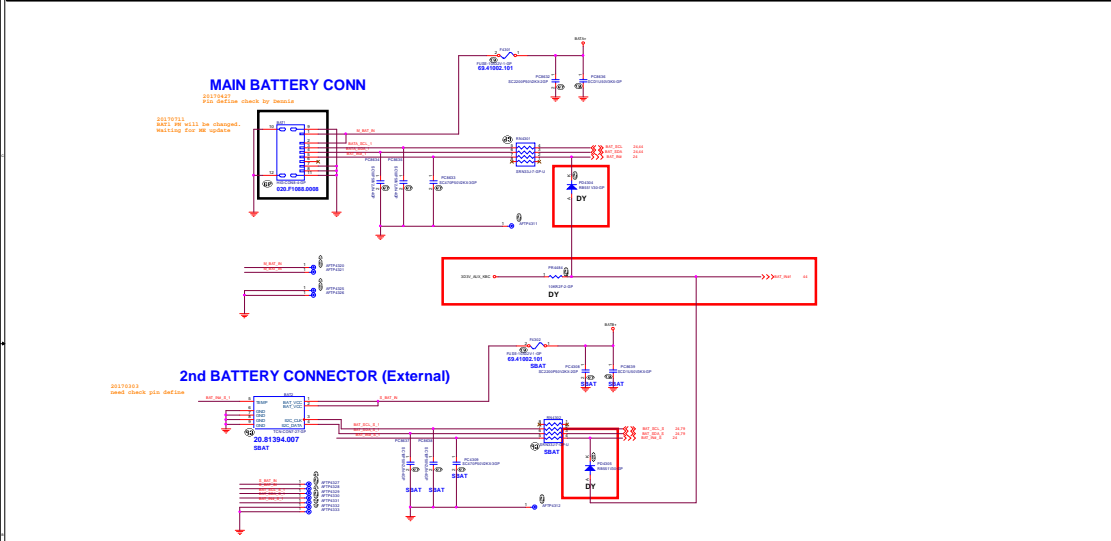
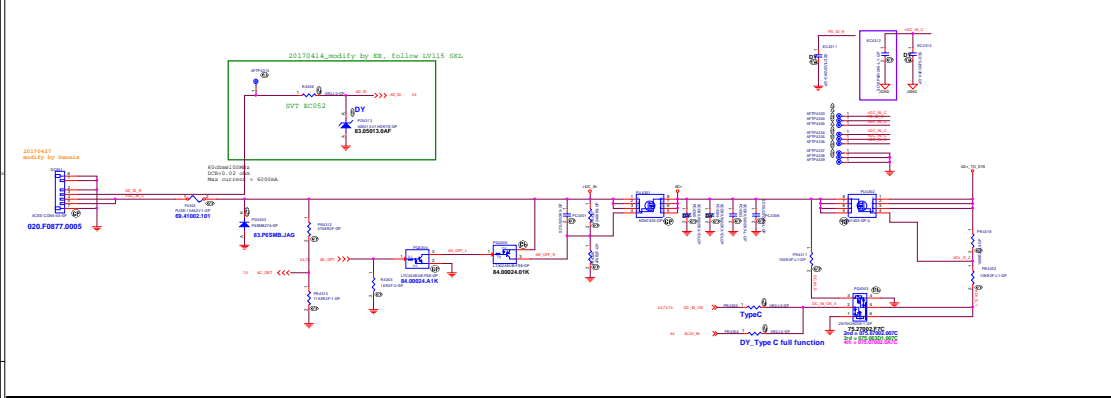
Document Number

Unicorn LV530 KBL MB GA

Rev

Date: Friday, December 15, 2017

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OFFPAGE Main Func = Charger

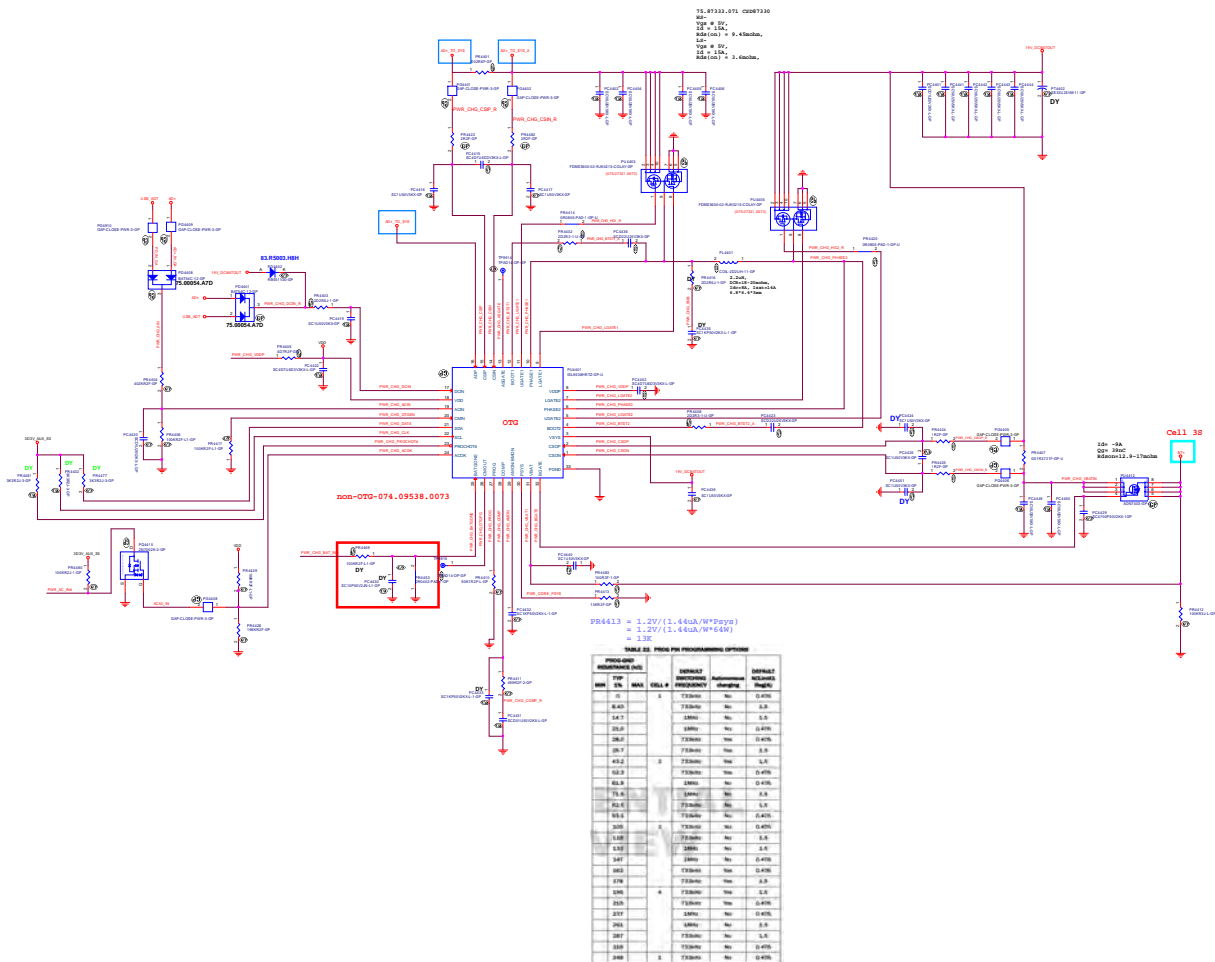
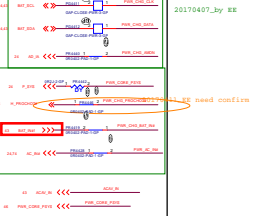
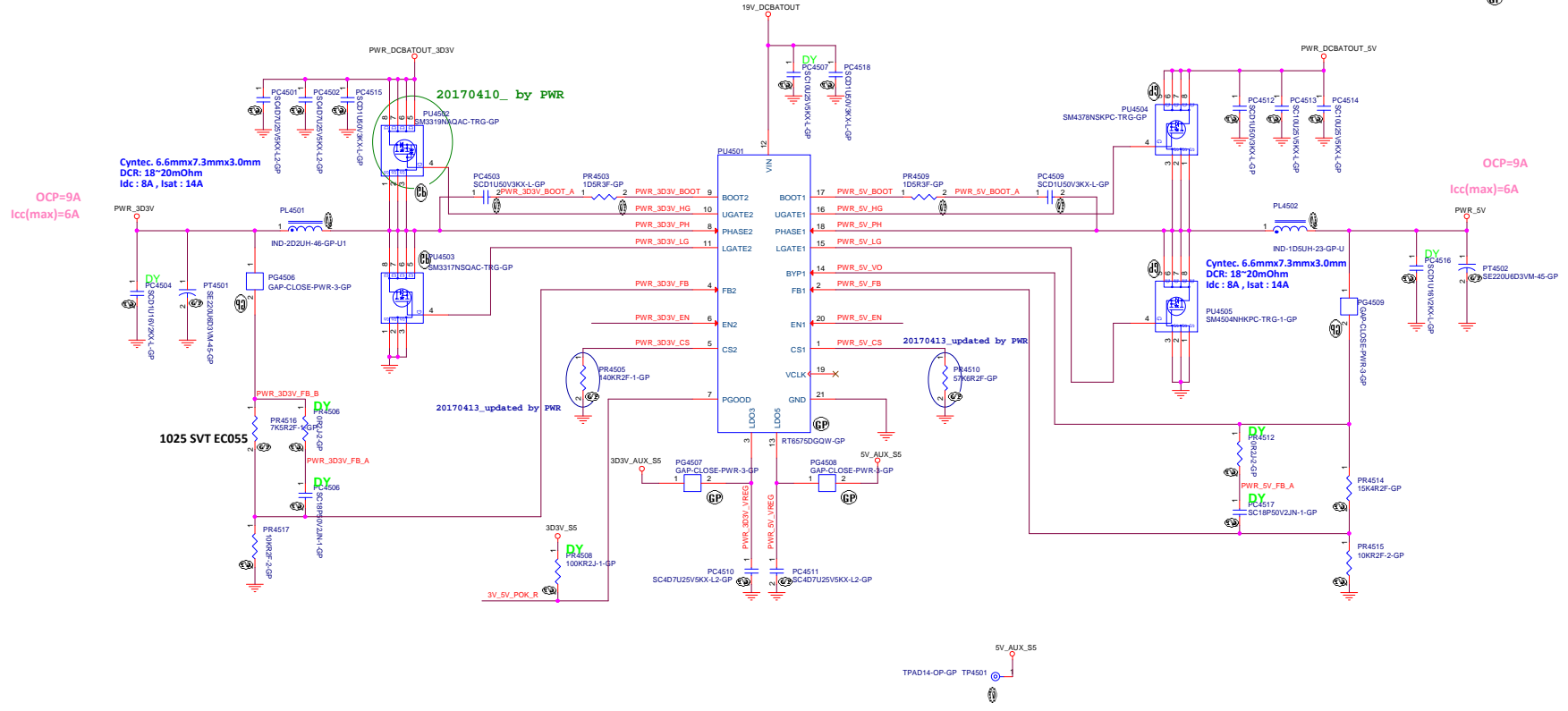
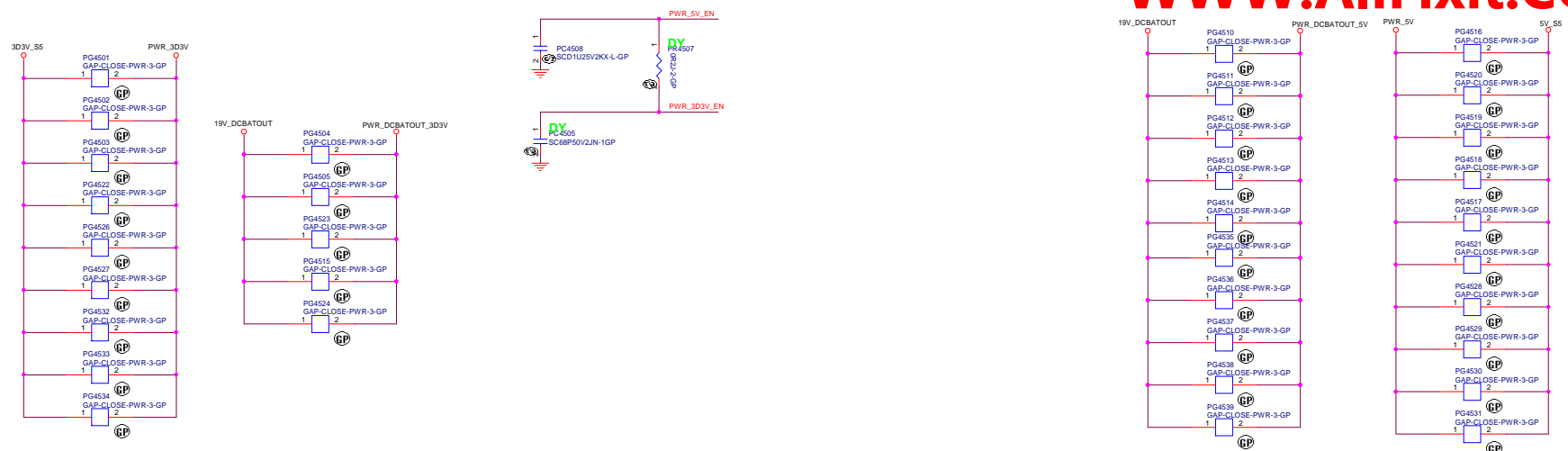
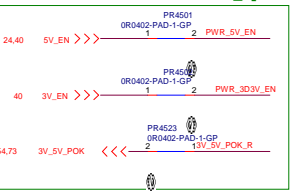


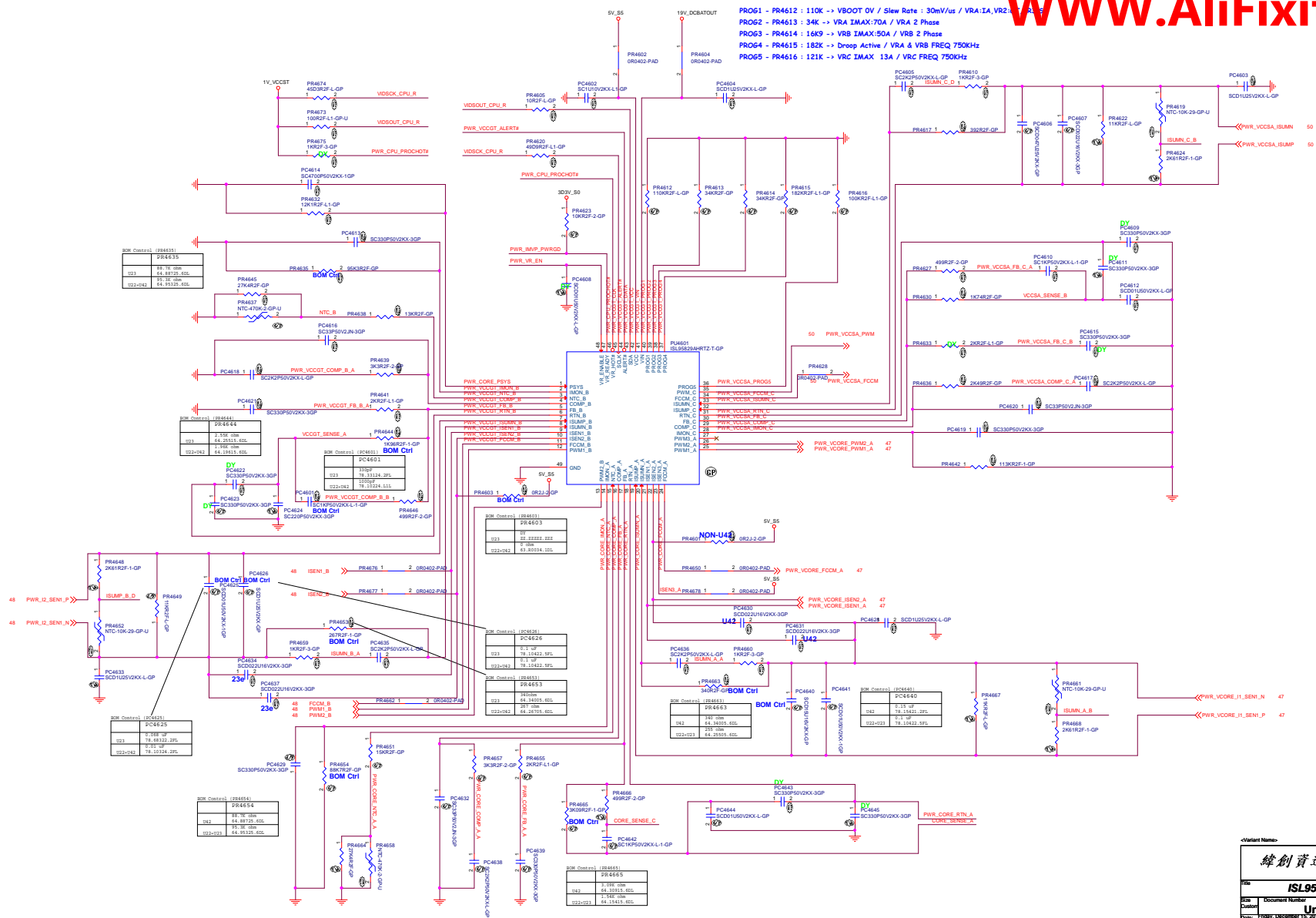
TABLE 22. PINS FOR PROGRAMMING OPTIONS

PROGRAMMING MODE	MIN	MAX	CH1.4	PROGRAMMING FREQUENCY	PROGRAMMING CURRENT	DEFAULT PROGRAMMING MODE
0	0	1	750uA	No	0.40V	0
6.45	1	750uA	No	0.5		6.45
6.47	1	750uA	No	0.5		6.47
28.0	1	750uA	No	0.40V		28.0
28.1	1	750uA	No	0.40V		28.1
28.7	1	750uA	No	0.5		28.7
43.2	1	750uA	No	0.5		43.2
62.3	1	750uA	No	0.40V		62.3
62.4	1	750uA	No	0.40V		62.4
62.5	1	750uA	No	0.5		62.5
62.6	1	750uA	No	0.5		62.6
62.7	1	750uA	No	0.40V		62.7
62.8	1	750uA	No	0.40V		62.8
62.9	1	750uA	No	0.40V		62.9
63.0	1	750uA	No	0.40V		63.0
63.1	1	750uA	No	0.40V		63.1
63.2	1	750uA	No	0.5		63.2
63.3	1	750uA	No	0.40V		63.3
63.4	1	750uA	No	0.40V		63.4
63.5	1	750uA	No	0.40V		63.5
63.6	1	750uA	No	0.40V		63.6
63.7	1	750uA	No	0.40V		63.7
63.8	1	750uA	No	0.40V		63.8
63.9	1	750uA	No	0.40V		63.9
64.0	1	750uA	No	0.40V		64.0
64.1	1	750uA	No	0.40V		64.1
64.2	1	750uA	No	0.40V		64.2
64.3	1	750uA	No	0.40V		64.3
64.4	1	750uA	No	0.40V		64.4
64.5	1	750uA	No	0.40V		64.5
64.6	1	750uA	No	0.40V		64.6
64.7	1	750uA	No	0.40V		64.7
64.8	1	750uA	No	0.40V		64.8
64.9	1	750uA	No	0.40V		64.9
65.0	1	750uA	No	0.40V		65.0
65.1	1	750uA	No	0.40V		65.1
65.2	1	750uA	No	0.40V		65.2
65.3	1	750uA	No	0.40V		65.3
65.4	1	750uA	No	0.40V		65.4
65.5	1	750uA	No	0.40V		65.5
65.6	1	750uA	No	0.40V		65.6
65.7	1	750uA	No	0.40V		65.7
65.8	1	750uA	No	0.40V		65.8
65.9	1	750uA	No	0.40V		65.9
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Wistron Corporation
 CHARGER(S142)HW72
 Unicorn LV530 KBL MS1500L

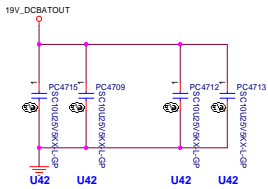
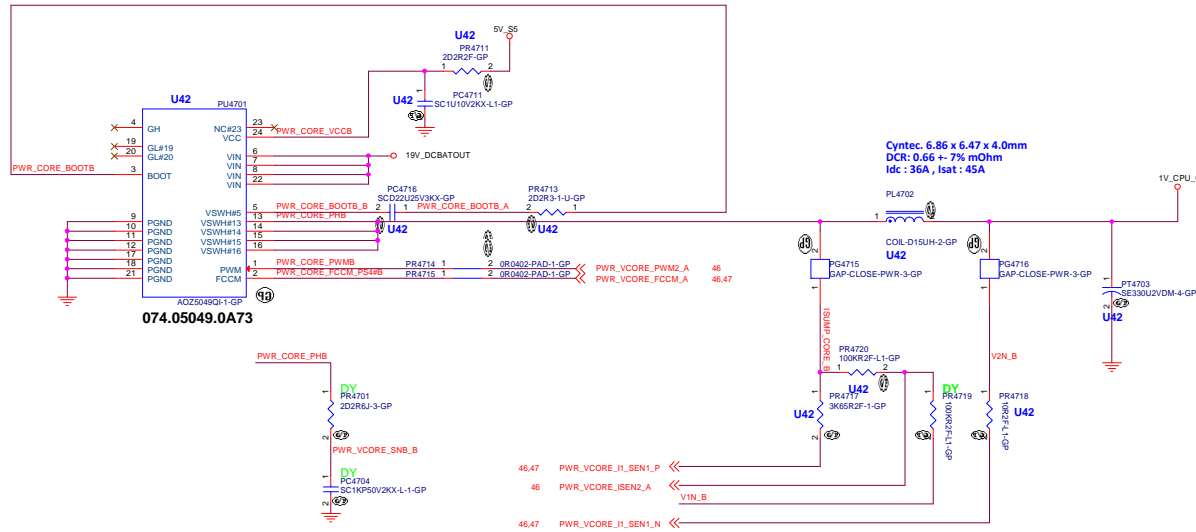
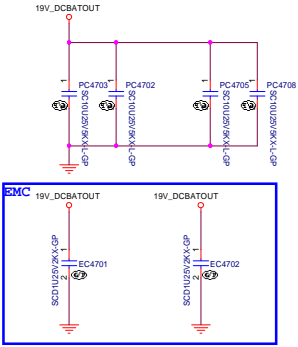
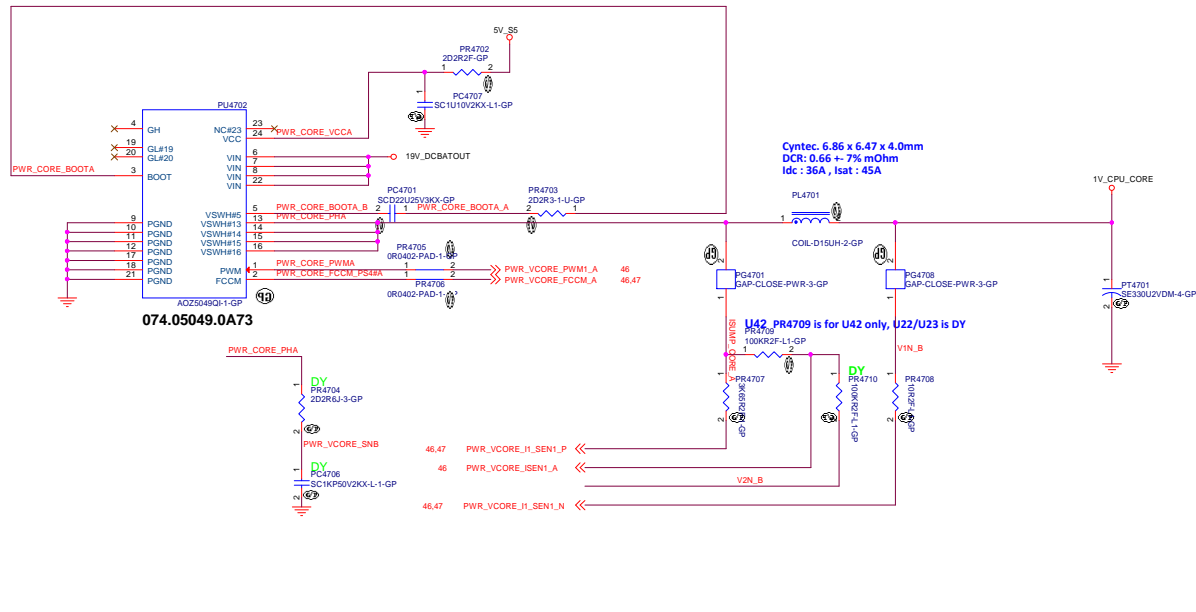


H_PROCHOT#	PR4656 1	2	PWR_CPU_PROCHOT#
	DR0402-PAD		
SVD_ALERT#_CPU	PR4608 1	2	PWR_VCCGT_ALERT#
	DR0402-PAD		
SVD_CLK_CPU	PR4621 1	2	VDSCK_CPU_R
	DR0402-PAD		
SVD_DATA_CPU	PR4618 1	2	VDSOUT_CPU_B
	DR0402-PAD		
VR_RDY	PR4640 1	2	PWR_MVP_PWRGD
	DR0402-PAD		
VR_EN	PR4641 1	2	PWR_VR_EN
	DR0402-PAD		
VBS_SENSE	PR4629 1	2	PWR_CORE_RTN_A
	DR0402-PAD		
VCC_SENSE	PR4671 1	2	CORE_SENSE_A
	DR0402-PAD		
VCCGT_SENSE	PR4606 1	2	VCCGT_SENSE_A
	DR0402-PAD		
VSSGT_SENSE	PR4607 1	2	PWR_VCCGT_RTN_B
	DR0402-PAD		
VSSA_SENSE	PR4629 1	2	PWR_VCCSA_RTN_C
	DR0402-PAD		
VCCSA_SENSE	PR4681 1	2	VCCSA_SENSE_B
	DR0402-PAD		
PWR_CORE_PSYS			PWR_CORE_PSYS



- PROG1 - PR4612 : 110K -> VBOOT OV / Slew Rate : 30mV/us / VRA:1A, VR2:1A, VR3:1A
- PROG2 - PR4613 : 34K -> VRA IMAX:70A / VRA 2 Phase
- PROG3 - PR4614 : 16K9 -> VRB IMAX:50A / VRB 2 Phase
- PROG4 - PR4615 : 182K -> Droop Active / VRA & VRB FREQ 750KHz
- PROG5 - PR4616 : 121K -> VRC IMAX 13A / VRC FREQ 750KHz

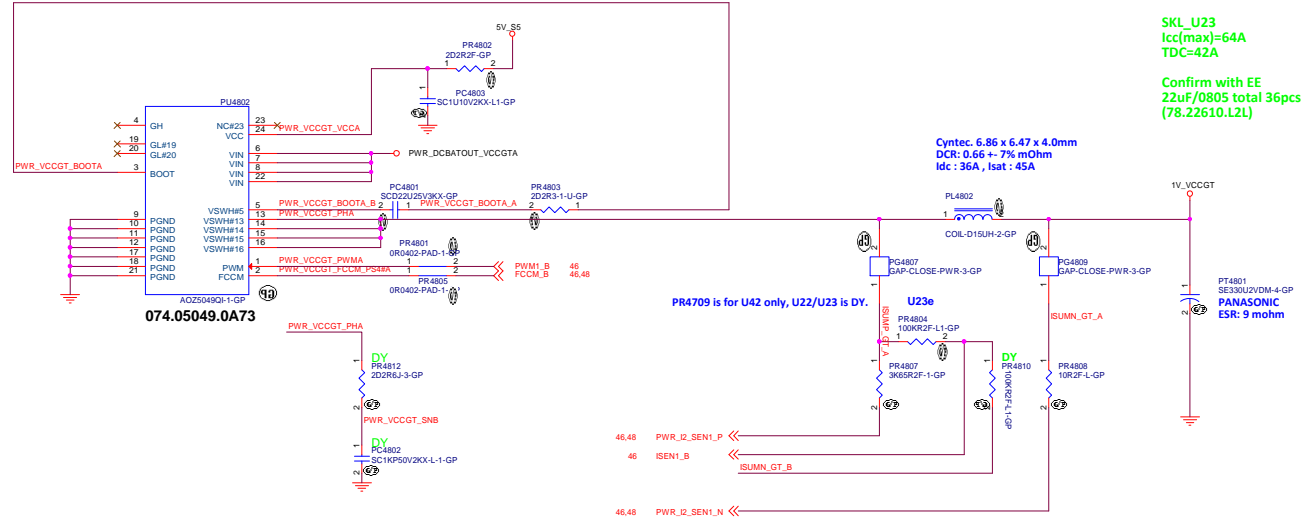
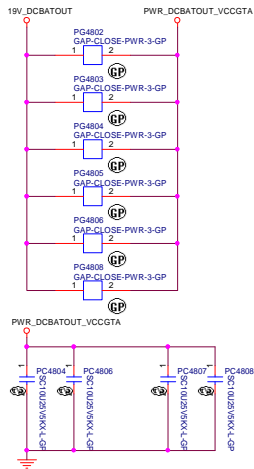
Wistron Corporation
 緯創資通
 31F, 6F, 5th Fl., Hsin-Tai Wu Rd., Hsinchu, Taipei Hsinchu 301, Taiwan, R.O.C.
 ISL95829 CPU_VCORE(1/3)
 Unicorn LV530 KBL MB PD
 Rev: 6/2015



Variant Name:

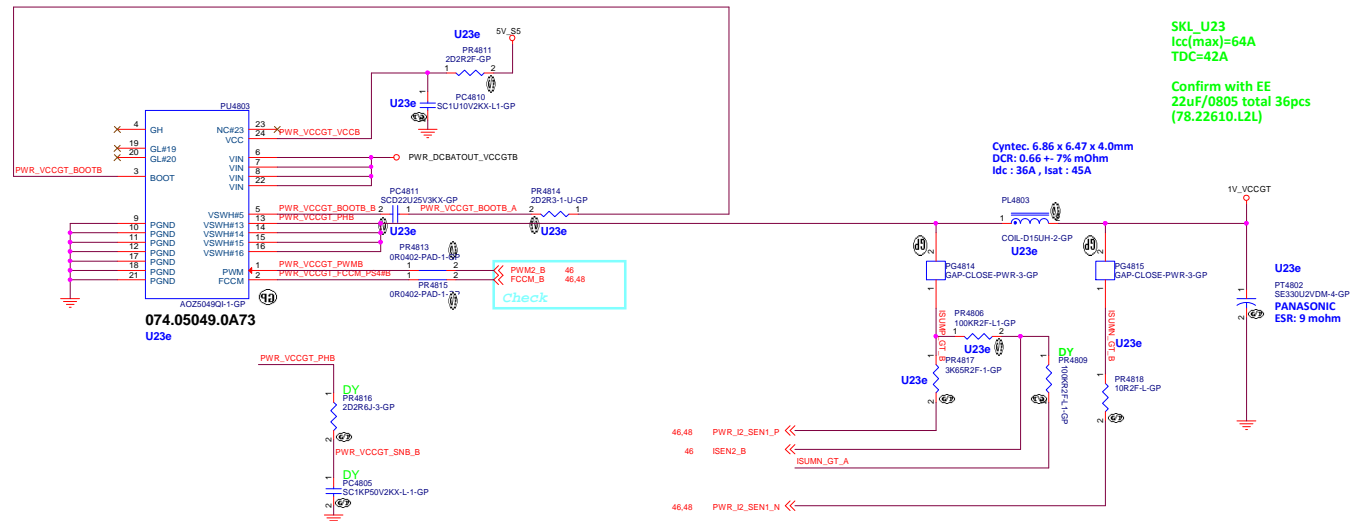
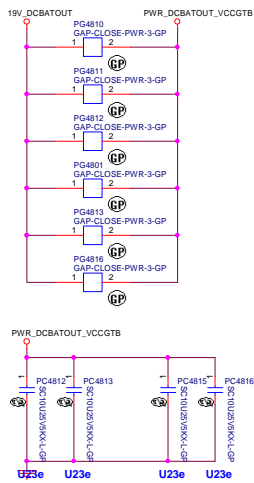
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

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Size	Document Number	Rev	
A2	Unicorn LV530 KBL MB		
Date:	Friday, December 16, 2017	Sheet	47 of 106



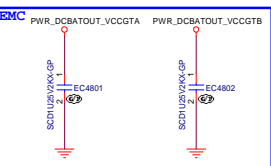
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Icc(max)=64A
TDC=42A

Confirm with EE
22uF/0805 total 36pcs
(78.22610.L2L)



SKL_U23
Icc(max)=64A
TDC=42A

Confirm with EE
22uF/0805 total 36pcs
(78.22610.L2L)



<Variant Name>

緯創資通 Wistron Corporation		21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsuehchu, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU_VCCGTUS		
Size	Document Number	Rev	
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Date:	Friday, December 15, 2017	Sheet	48 of 106

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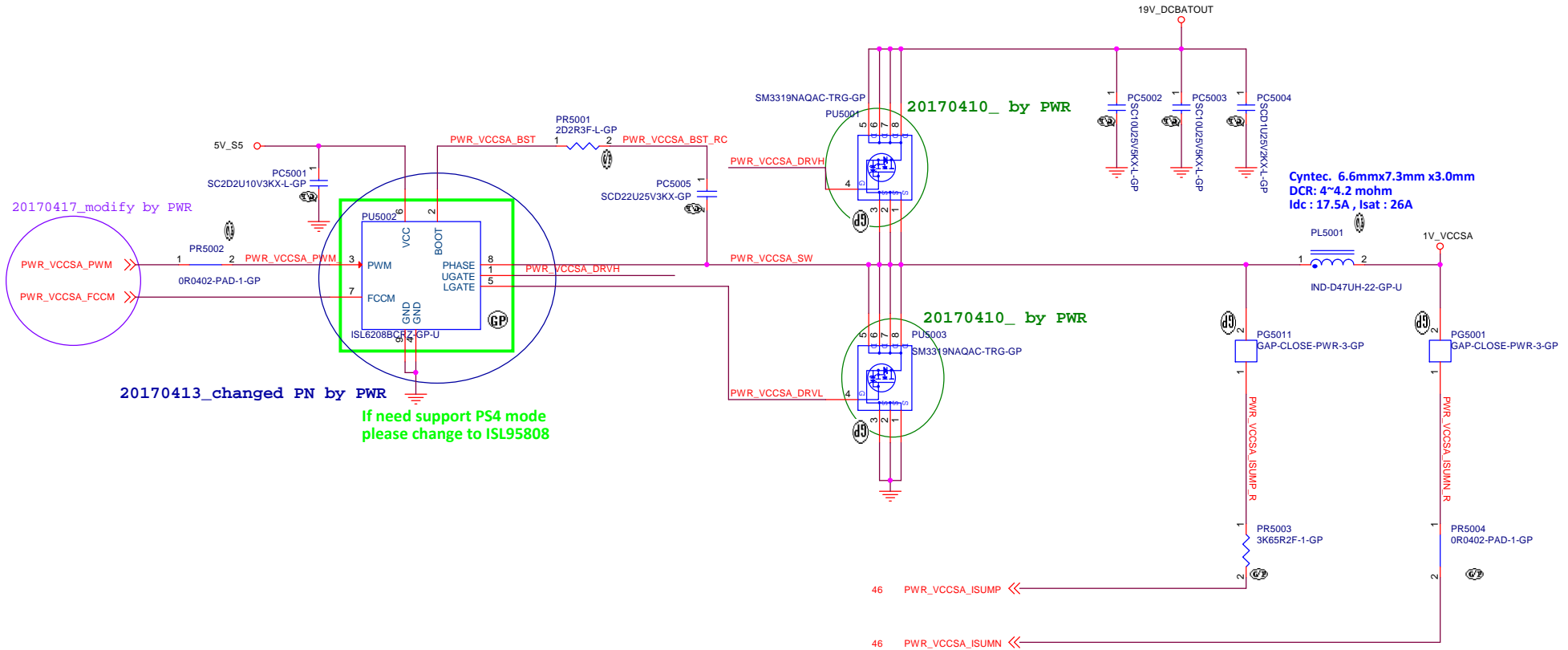
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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **CPU_VCCGTUS**

Size A4	Document Number Unicorn LV530 KBL MB GA	Rev GA
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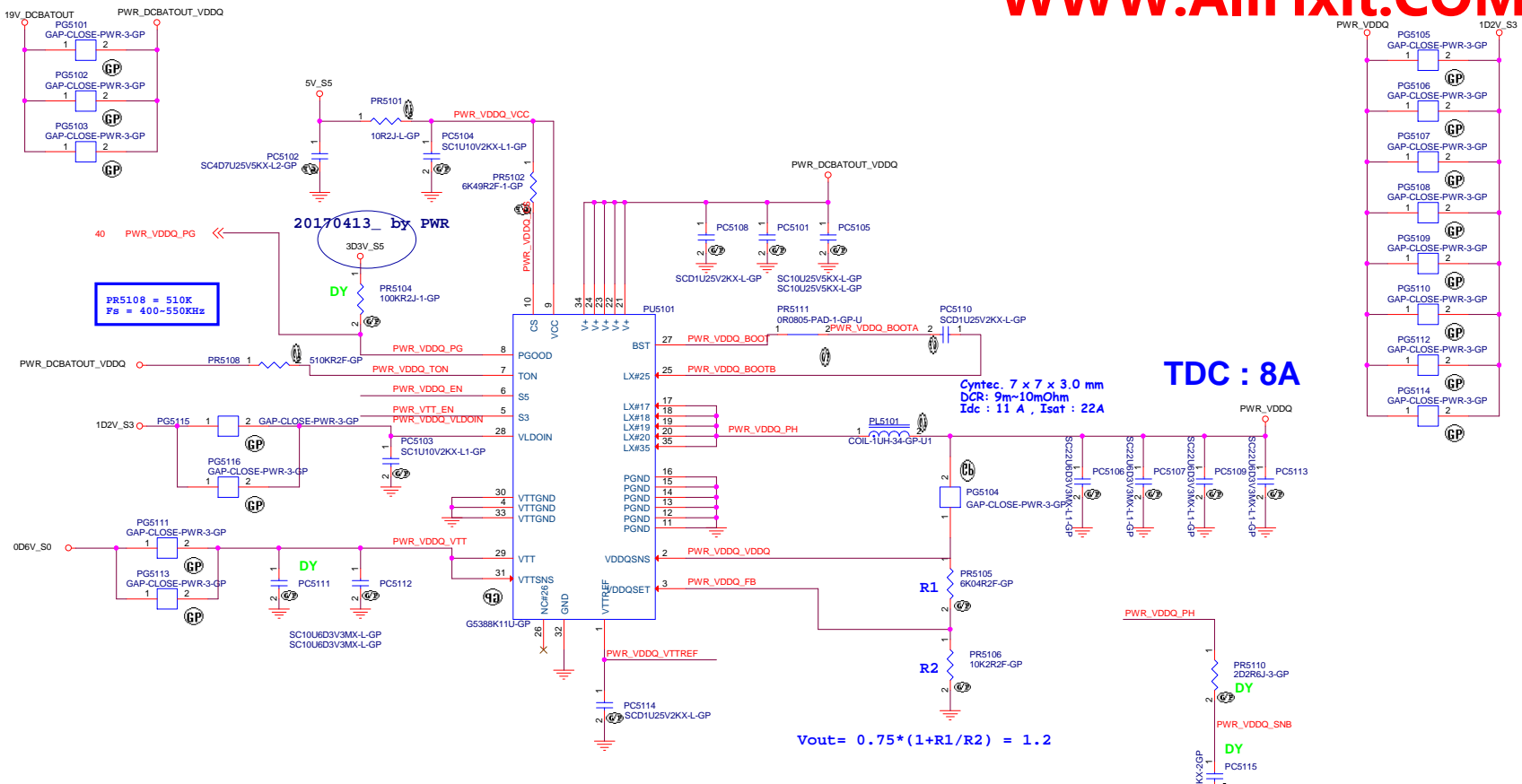
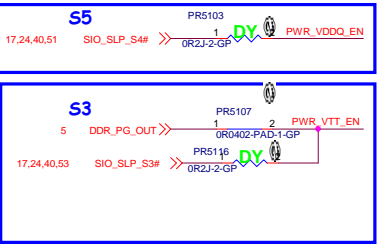
Date: Friday, December 15, 2017 Sheet 49 of 105



Cyntec. 6.6mmx7.3mm x3.0mm
 DCR: 4~4.2 mohm
 Idc : 17.5A, Isat : 26A

<small><Variant Name></small>		
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	CPU_VCCGTUS	
Size	Document Number	Rev
A3	Unicorn LV530 KBL MB14A	
Date:	Friday, December 15, 2017	Sheet 50 of 105

OFFPAGE



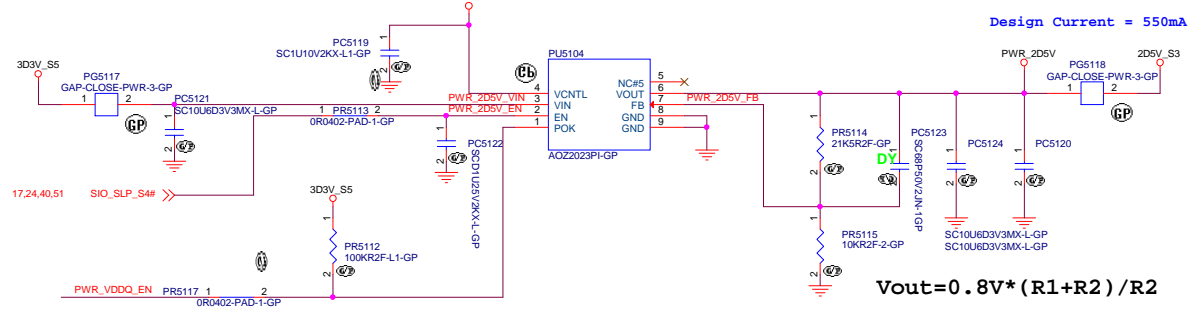
20170413 by PWR
3D3V_S5
PR5108 = 510K
Fs = 400-550KHz

TDC : 8A

Cyntec, 7 x 7 x 3.0 mm
DCR: 9m-10mOhm
Idc : 11 A , Isat : 22A

$V_{out} = 0.75 * (1 + R1/R2) = 1.2$

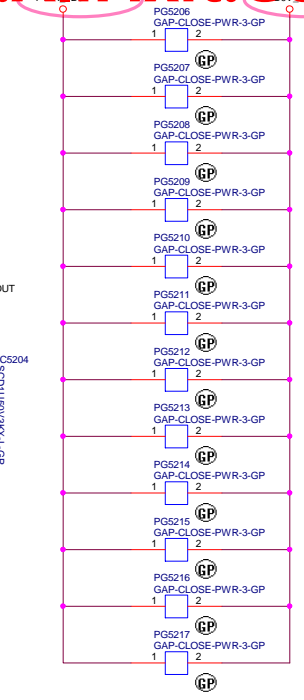
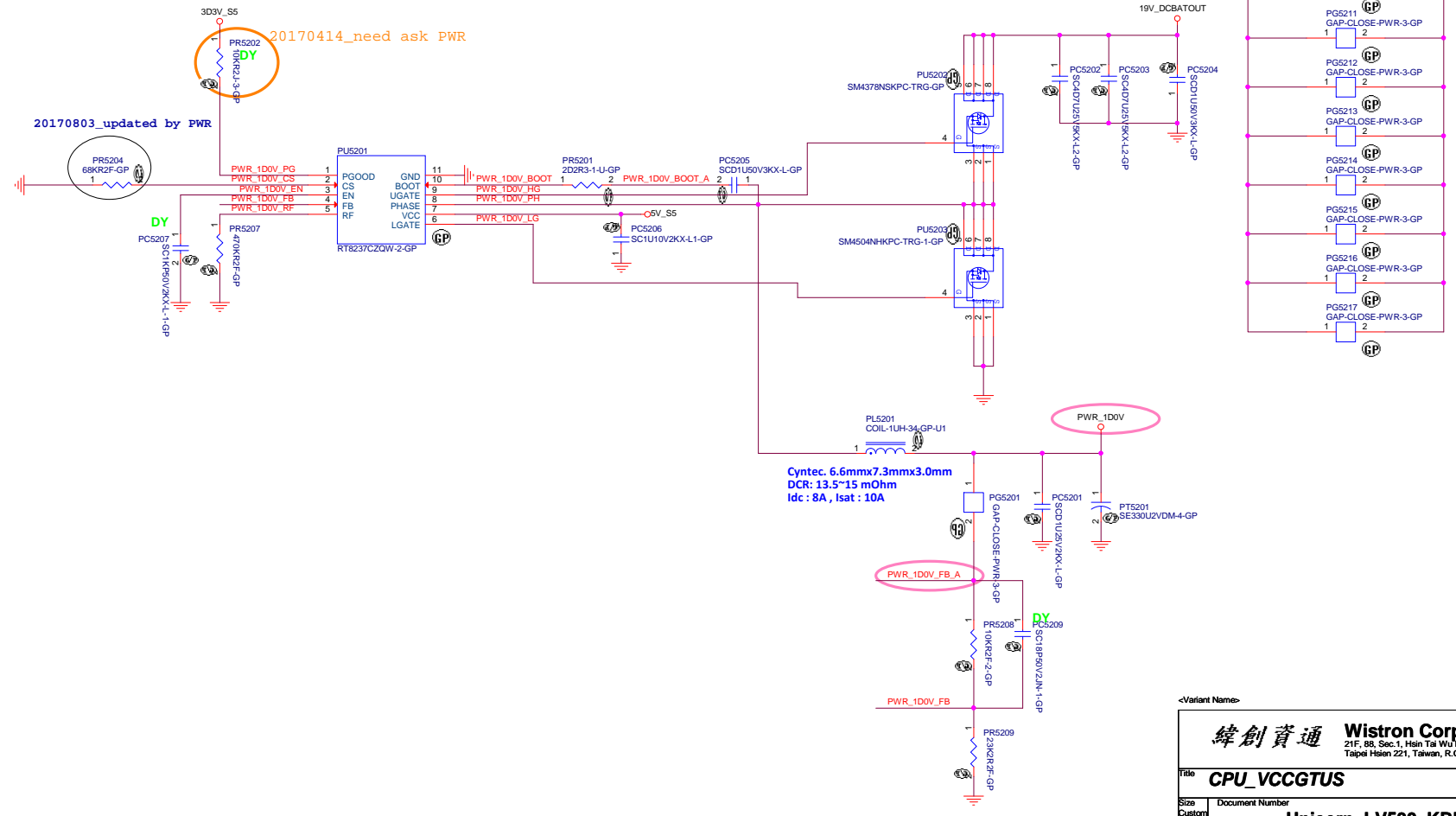
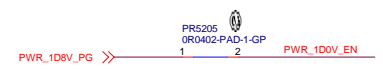
RT9025 for 2D5V



$V_{out} = 0.8V * (R1+R2) / R2$

BOM1

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: G5388_VDDQ	
Size: Custom	Document Number: Unicorn LV530 KBL MB18A
Date: Friday, December 15, 2017	Sheet: 51 of 105



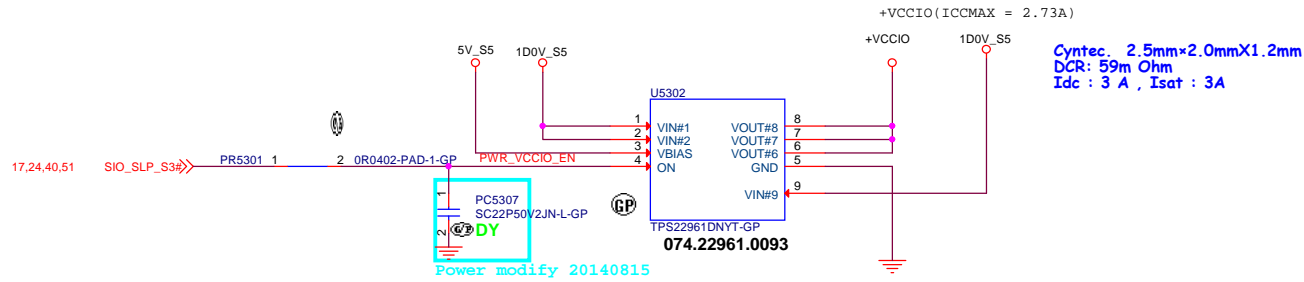
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Trd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

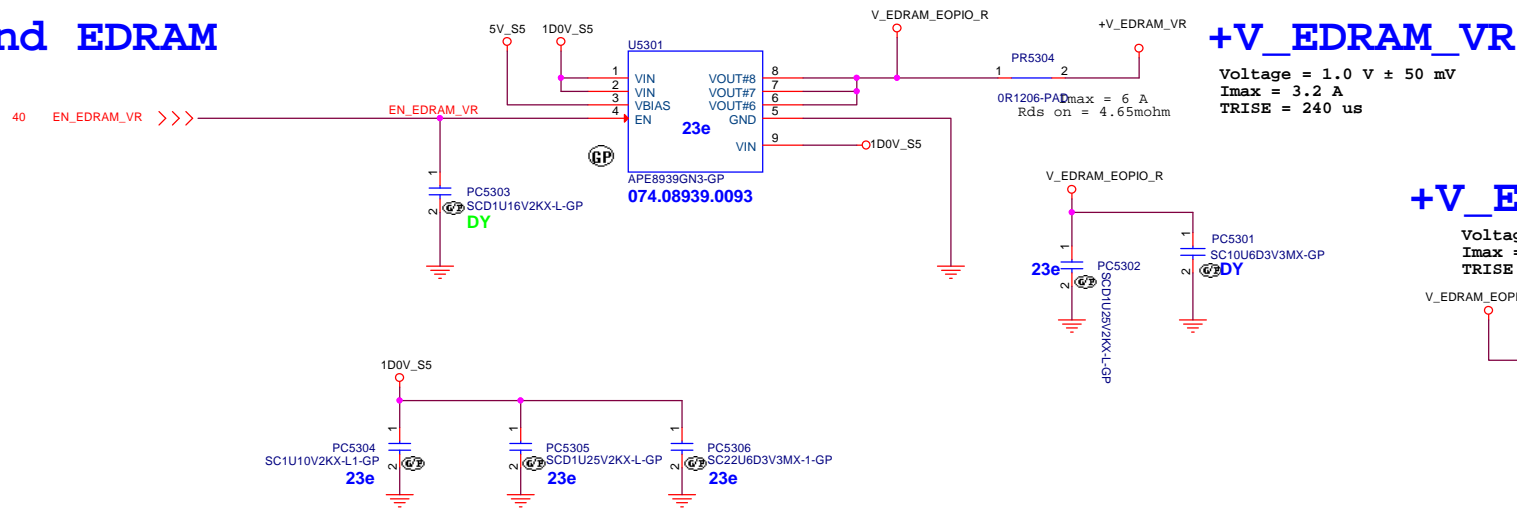
File	CPU_VCCGTUS		
Size	Document Number	Rev	
Custom	Unicorn LV530 KBL MB14A		
Date:	Friday, December 15, 2017	Sheet 52	of 105

Main Func = 1D0V

VCCIO



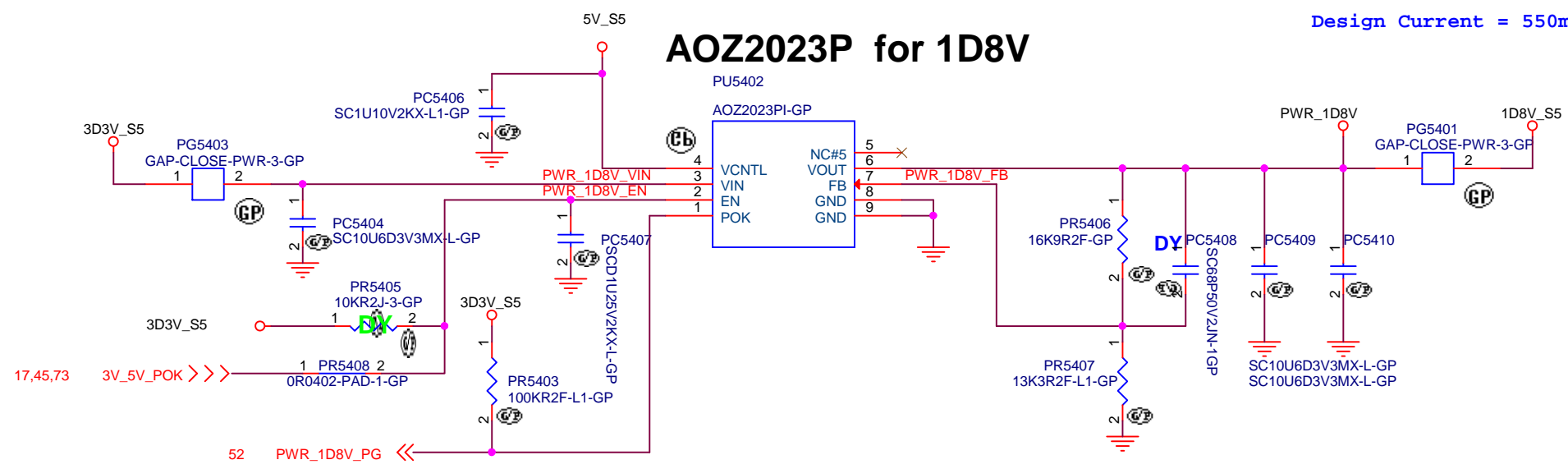
EOPIO and EDRAM



<Variant Name>		
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title TPS2296 VCCIO&VCCPRIM		
Size A3	Document Number Unicorn_LV530_KBL_MB14	Rev SA
Date: Friday, December 15, 2017	Sheet 53	of 105

Main Func = 1D8V

WWW.AliFixit.COM



AOZ2023P for 1D8V

Design Current = 550mA

$$V_{out} = 0.8V * (R1 + R2) / R2$$

<Variant Name>

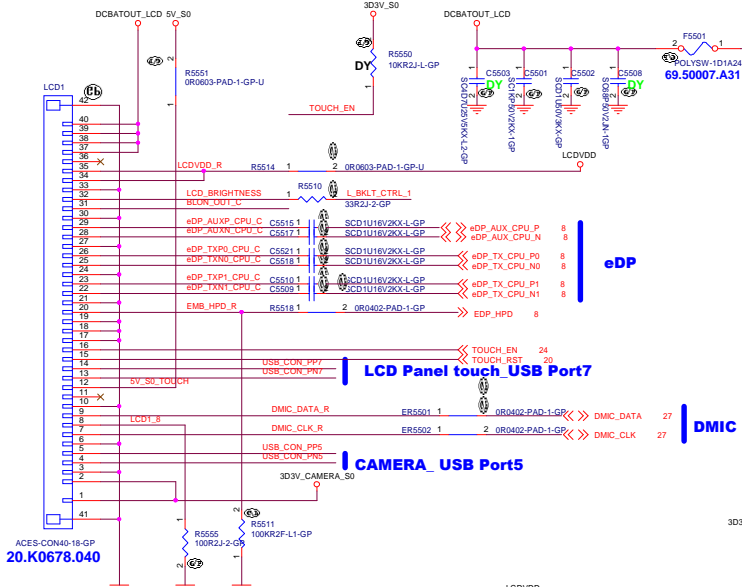
緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		
RT9025 1D8V		
Size	Document Number	Rev
A4	Unicorn LV530 KBL MB GA	
Date:	Friday, December 15, 2017	Sheet 54 of 105

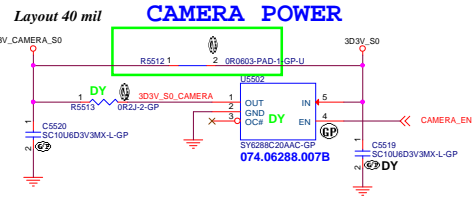
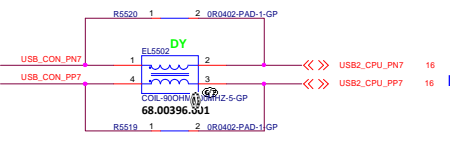
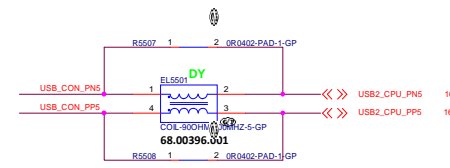
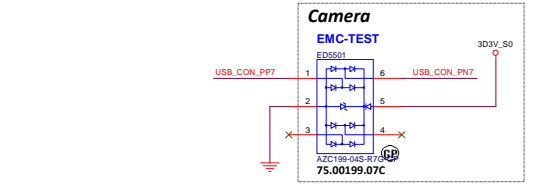
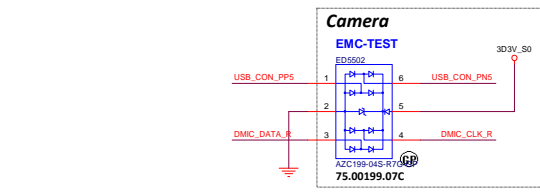
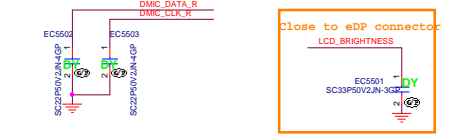
WWW.ALISALER.COM

SSID = VIDEO eDP connector

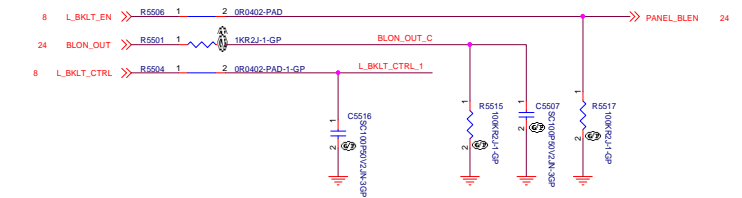
20170427 need check pin define



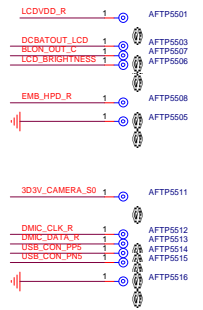
2) 3 empty pins between wire cable(MIC, camera, or other control signals) & coaxial cable(LCD panel usage). (Apply to LNB only)



Panel BL brightness/Power En/BL En



Test point



Shark Bay SV

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
ODD(Reserved)			
Size	Document Number	Rev	
A3			Unicorn LV530 KBL MB13A
Date:	Friday, December 15, 2017	Sheet	56 of 105

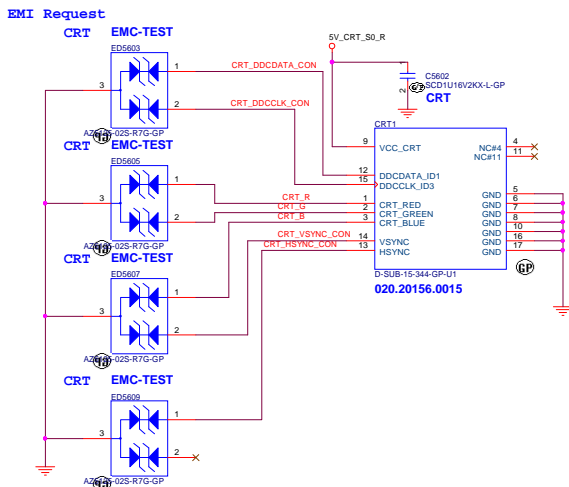
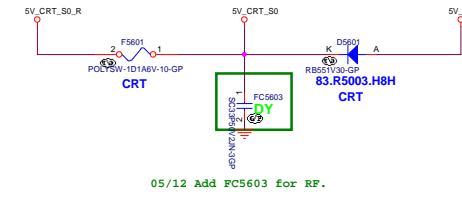
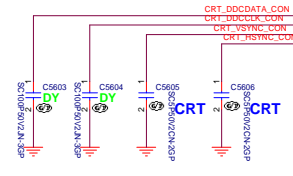
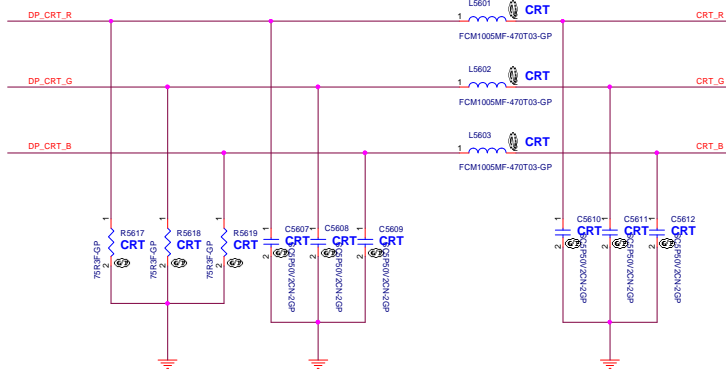


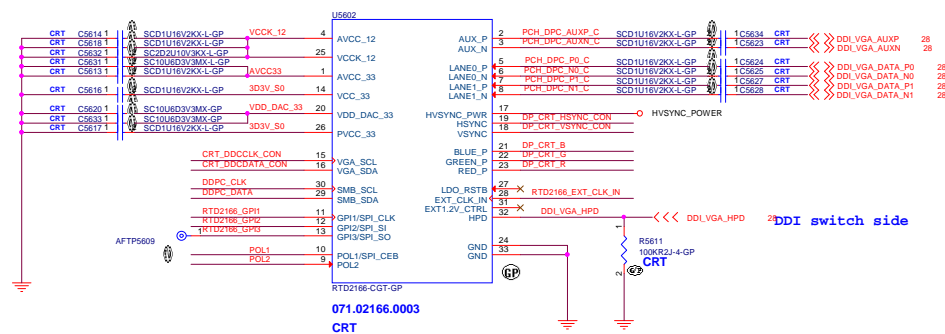
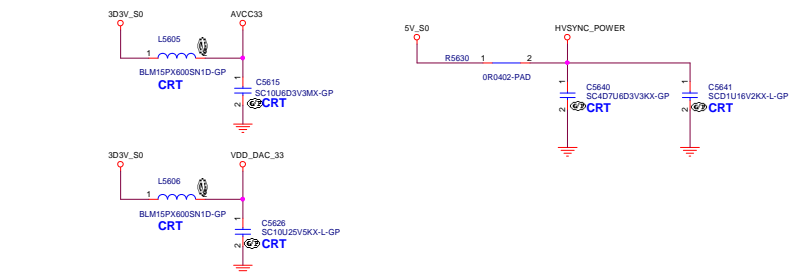
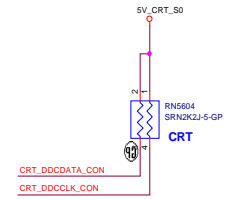
Table listing component values for CRT signals: 5V_CRT_S0_R (1), CRT_DDCCDATA_CON (1), CRT_DDCCCLK_CON (1), CRT_R (1), CRT_G (1), CRT_B (1), CRT_VSYNC_CON (1), CRT_HSYNC_CON (1), and AFTP5601 through AFTP5608.



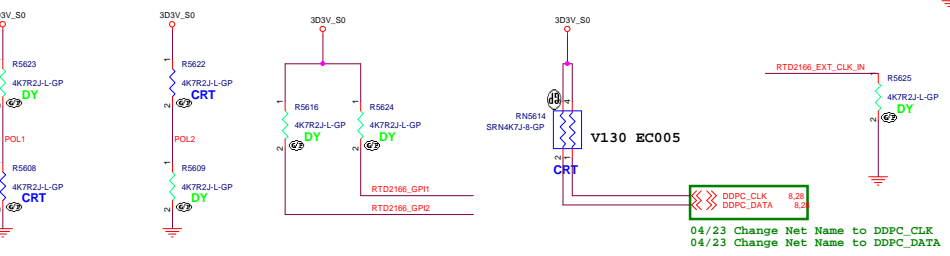
05/12 Add FC5603 for RF.



LAYOUT NOTE: All cap need close to chip especially C616 close pin5, C618 and C619 close pin19, C620 and C621 close pin9, C617 close pin20, C614 close pin25, C613 lose pin24



DDI switch side



04/23 Change Net Name to DDPC_CLK
04/23 Change Net Name to DDPC_DATA

(Blank)

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size
A4

Document Number

Unicorn LV530 KBL MB SA

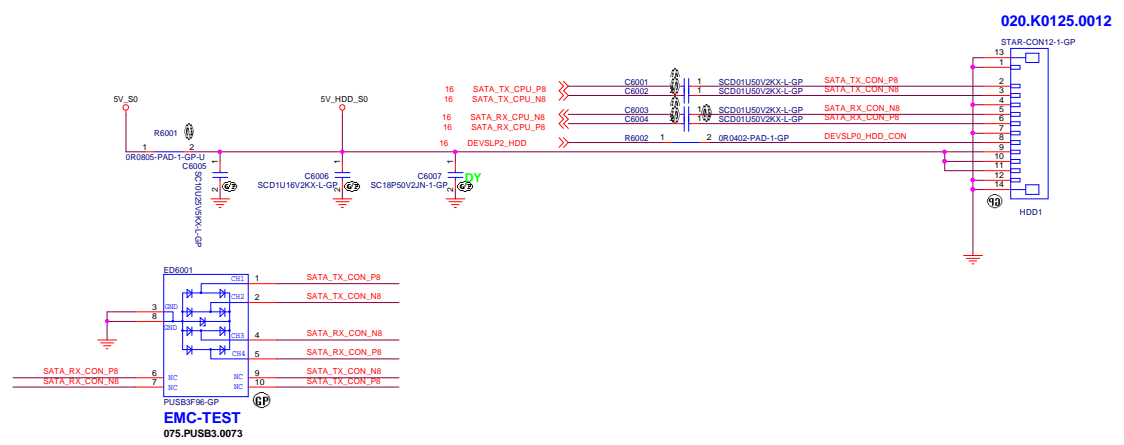
Rev

Date: Friday, December 15, 2017

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HDD 20170427

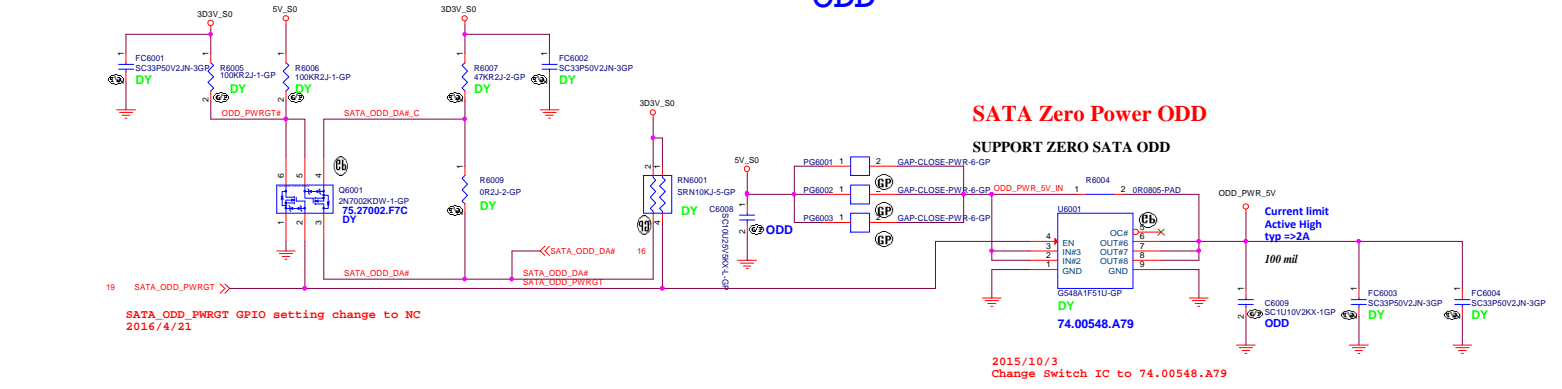
Change pin define follow LV315ST(NC) but pn 1 different



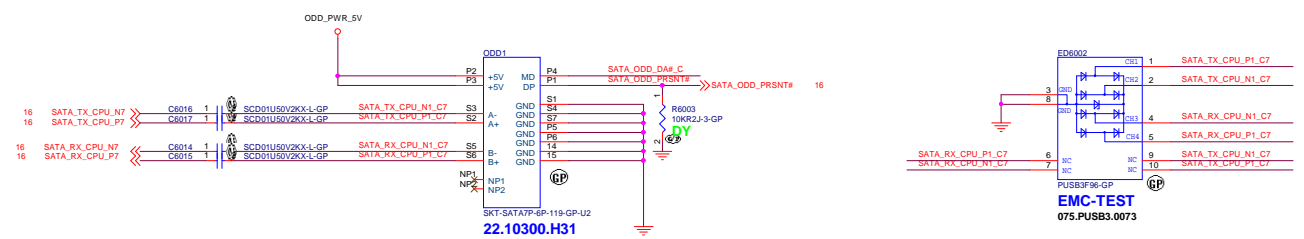
ODD

SATA Zero Power ODD

SUPPORT ZERO SATA ODD



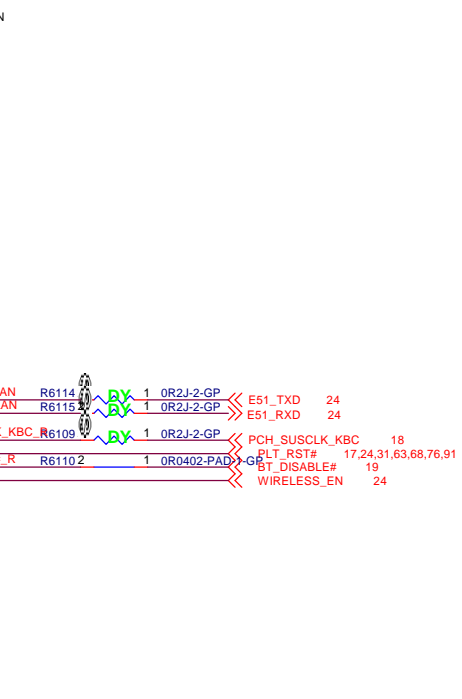
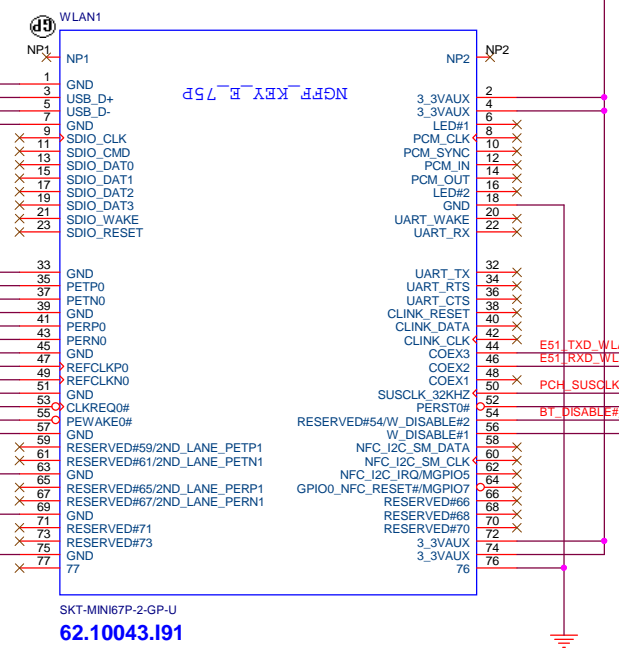
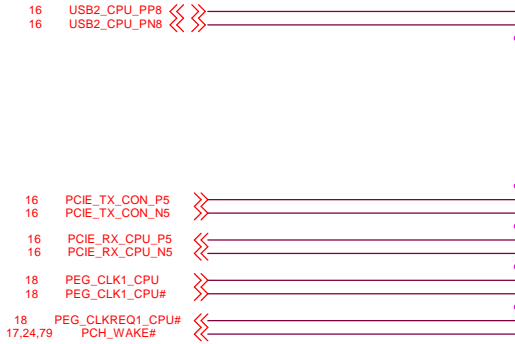
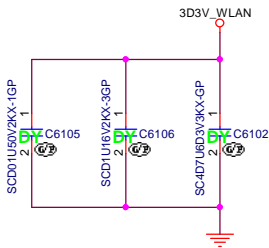
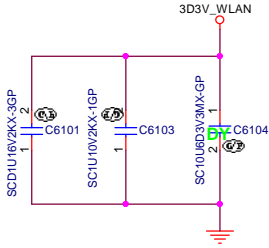
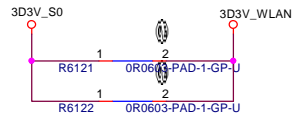
2015/10/3
Change Switch IC to 74.00548.A79



Main Func = WLAN

M.2 Key-E FOR WLAN / BT

2.5A peak
1.1A Cont



SKT-MINI67P-2-GP-U
62.10043.I91

BOM1

緯創資通 Wistron Corporation
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Title: **NGFF WLAN CONN**

Size: A3	Document Number: Unicorn LV530 KBL MB14	Rev: SA
Date: Friday, December 15, 2017	Sheet: 61	of 105

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BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size
A4

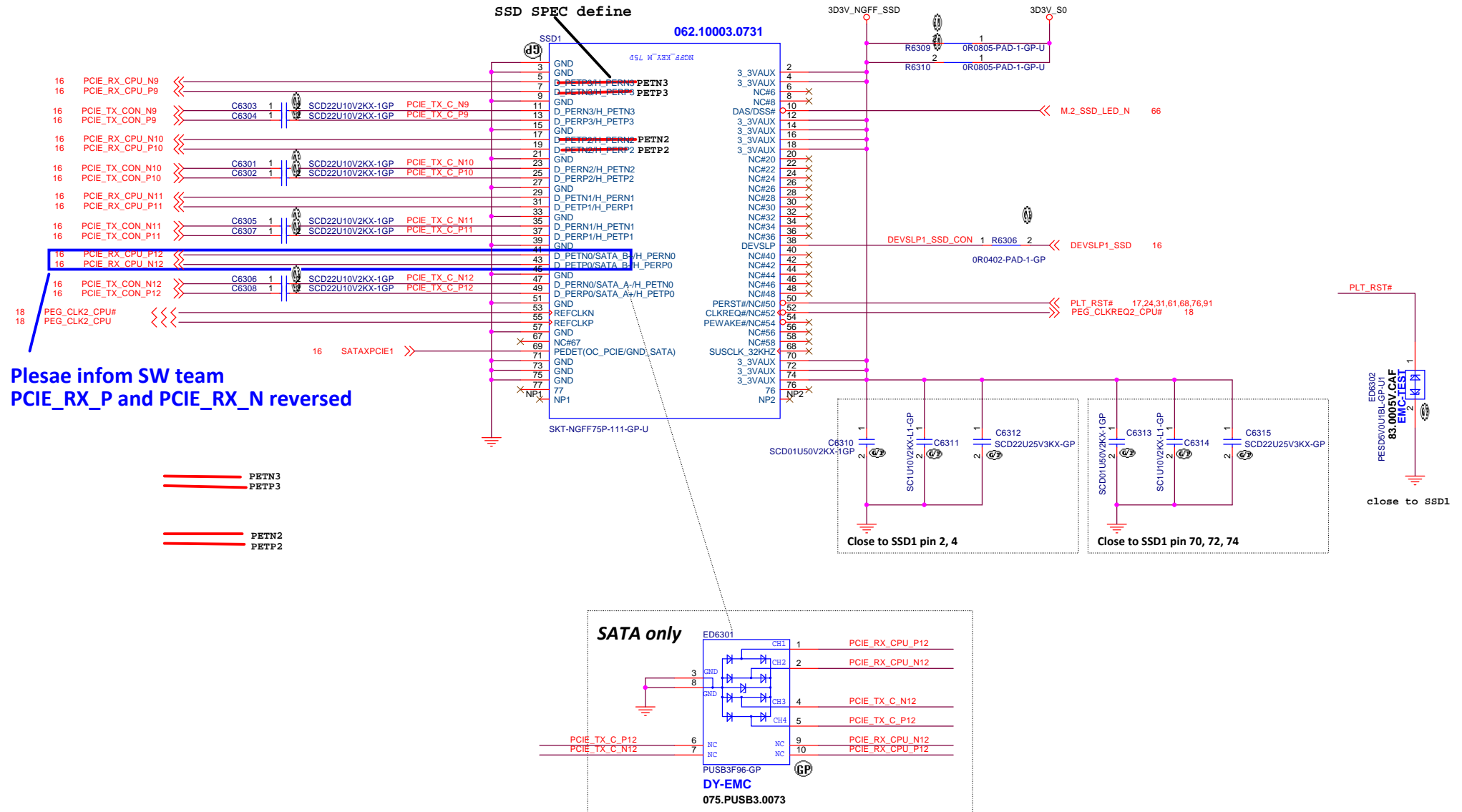
Document Number

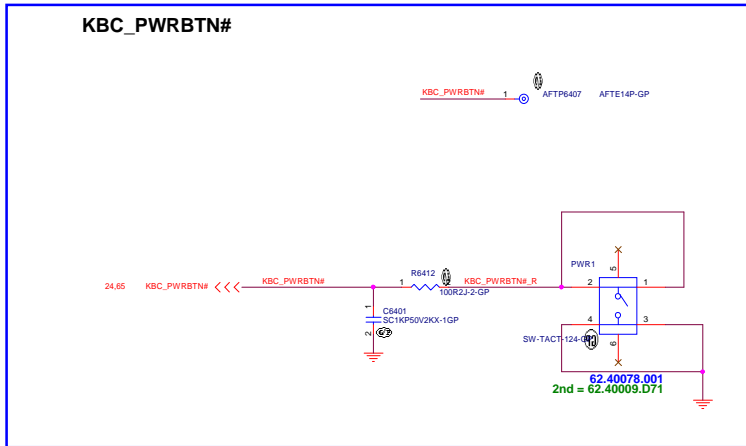
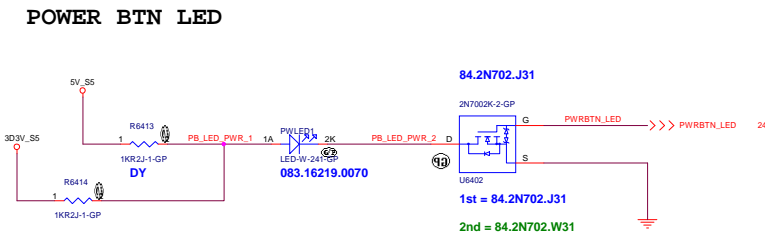
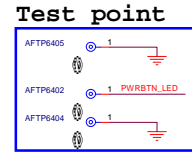
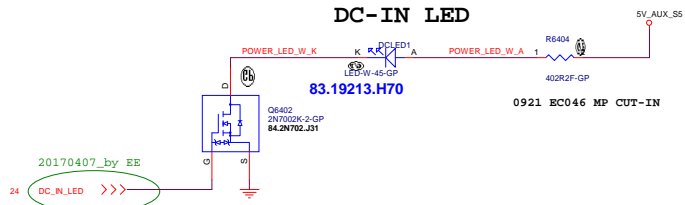
Unicorn LV530 KBL MB GA

Rev

Date: Friday, December 15, 2017

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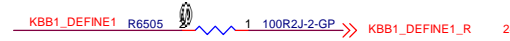
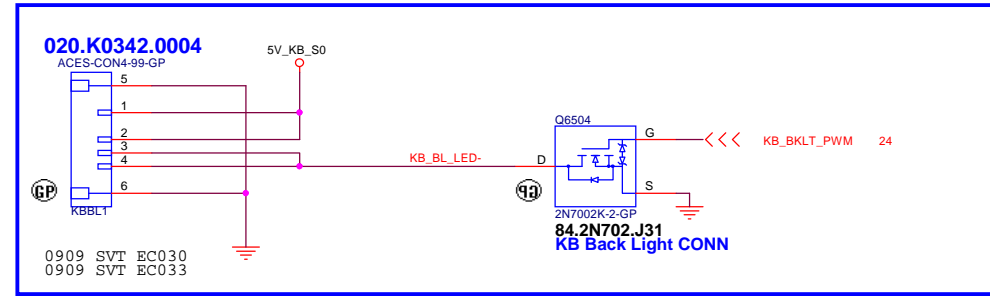
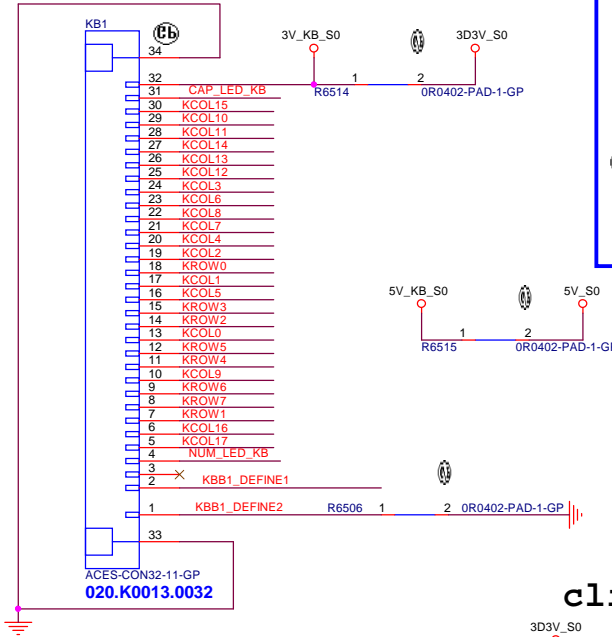
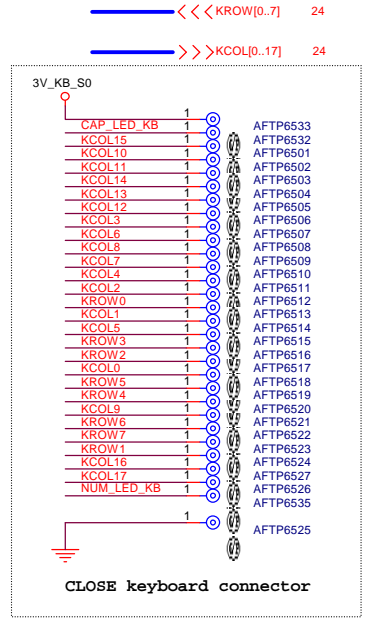




SSID = Touch.Pad

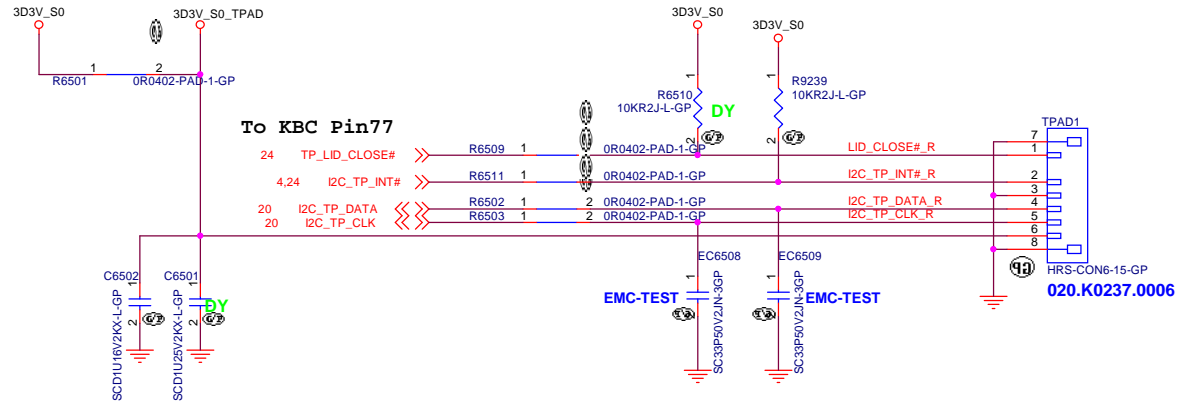
20170427_pin deifne check by Dennis

KB_LED

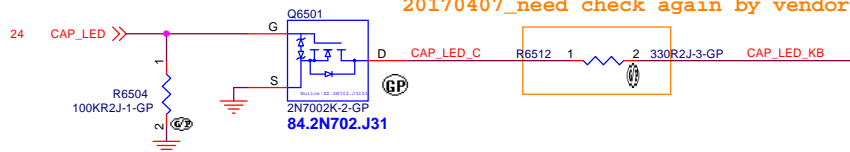


20170421 Cnhange pin deifne by Dennis

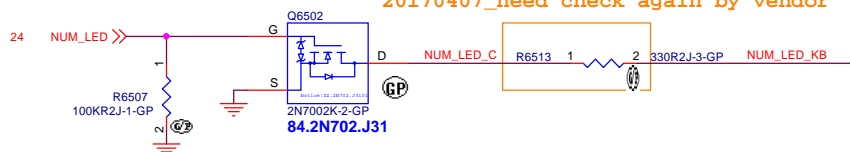
click pad



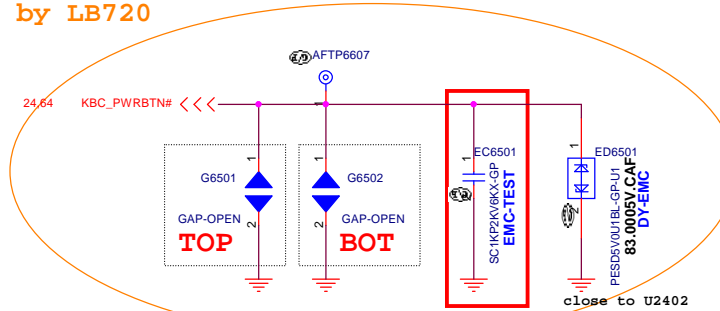
20170407_need check again by vendor



20170407_need check again by vendor



20170412_WKS test by LB720

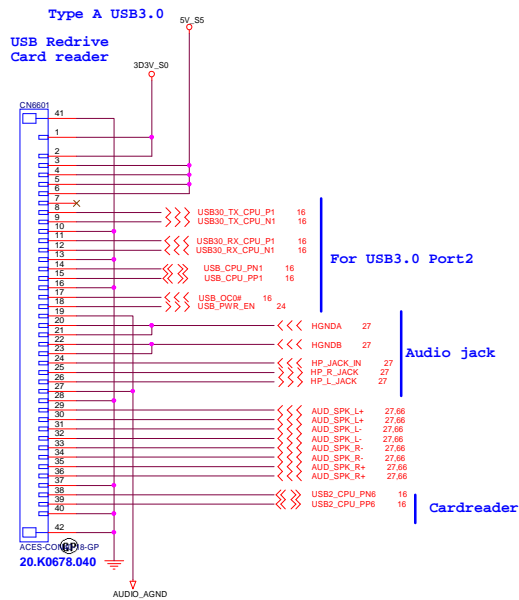


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

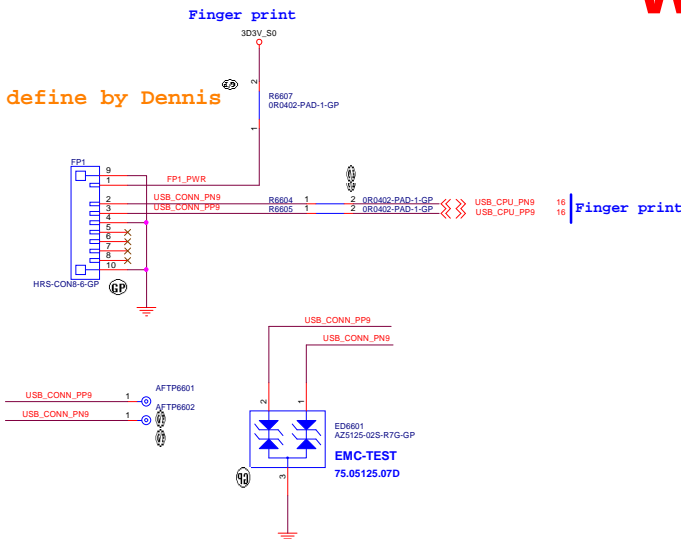
Title: **KEYBOARD/TOUCH PAD**

Size A3 Document Number: **Unicorn LV530 KBL MB14** Rev SA

Date: Friday, December 15, 2017 Sheet 65 of 105

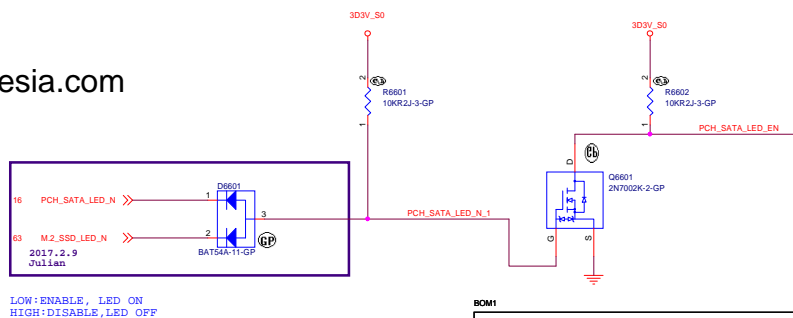
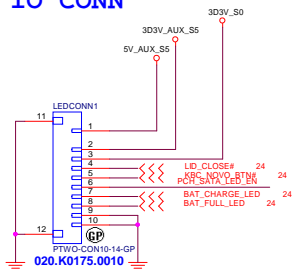


20170421
Change pin define by Dennis



LED IO CONN

www.teknisi-indonesia.com



LOW:ENABLE, LED ON
HIGH:DISABLE,LED OFF

BOM1

Wistron Corporation 2/F, 88, Sec.1, Hsin-Tsa WU Rd., Hsuehshin, Taipei Hsien 221, Taiwan, R.O.C.	
Title: LEDIO IO BOARD CONN	
Size: A2	Document Number: Unicom LV530_KBL_MB14
Date: Friday, December 15, 2017	Rev: SA
Sheet: 66 of 105	

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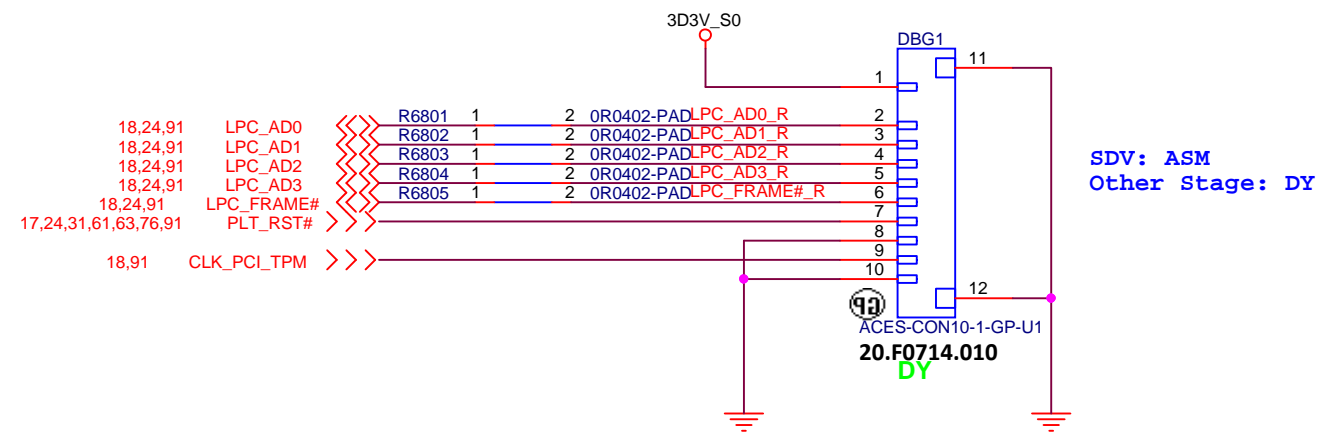
BOM1

緯創資通		Wistron Corporation
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
RESERVED		

Size A4	Document Number Unicorn LV530 KBL MB GA	Rev
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Debug Connector



BOM1

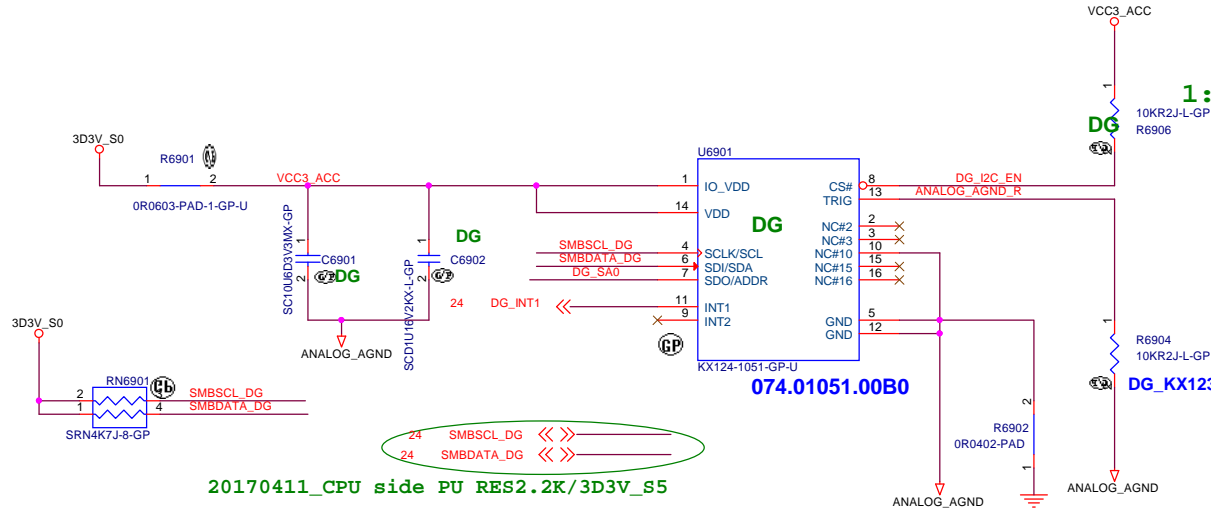
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **DEBUG CONN**

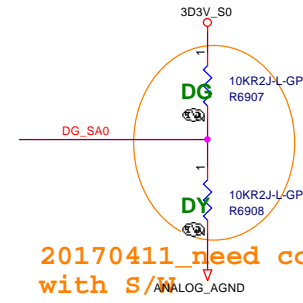
Size A4	Document Number	Rev SA
Unicorn_LV530_KBL_MB14		

G-Sensor

1st:ST/ LIS3DETR, 74.00003.BB0
(cannot be used, bit not enough)
2nd:KX124-1051, 074.01051.00B0



1: I2C communication enable



20170411_need confirm address with S/M

20170411_CPU side PU RES2.2K/3D3V_S5

(Blank)

BOM1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size
A4

Document Number

Unicorn LV530 KBL MB GA

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BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title

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Size
A4

Document Number

Unicorn LV530 KBL MB GA

Rev

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BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title

RESERVED

Size
A4

Document Number

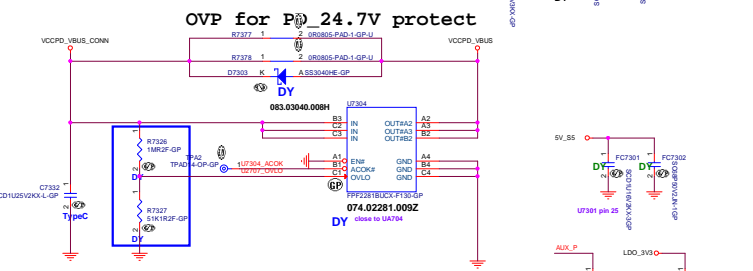
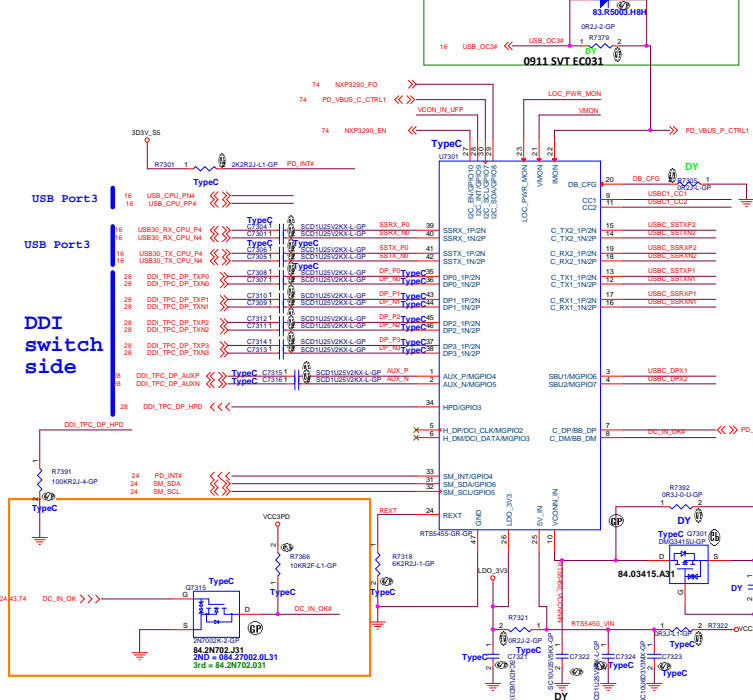
Unicorn LV530 KBL MB GA

Rev

Date: Friday, December 15, 2017

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USB Port4, Type C_USB3.0, PD, DP

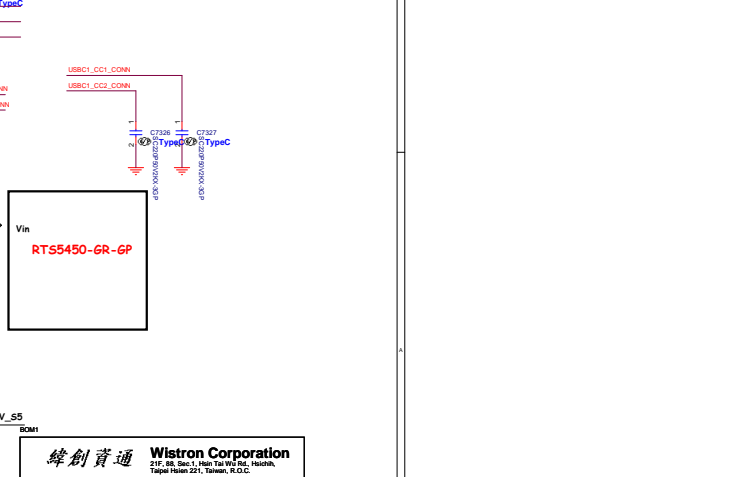
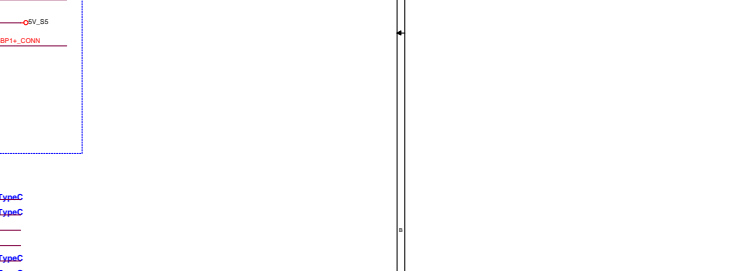
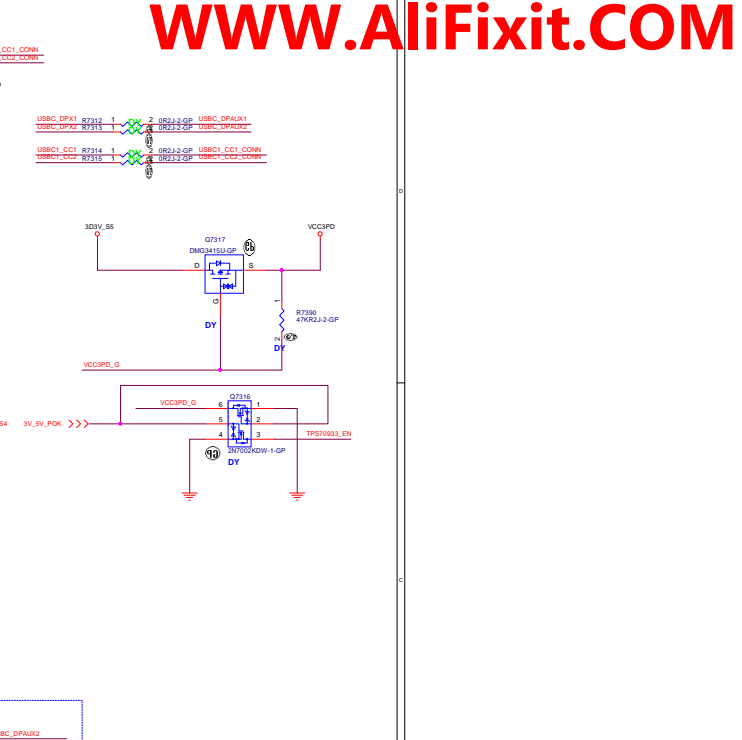
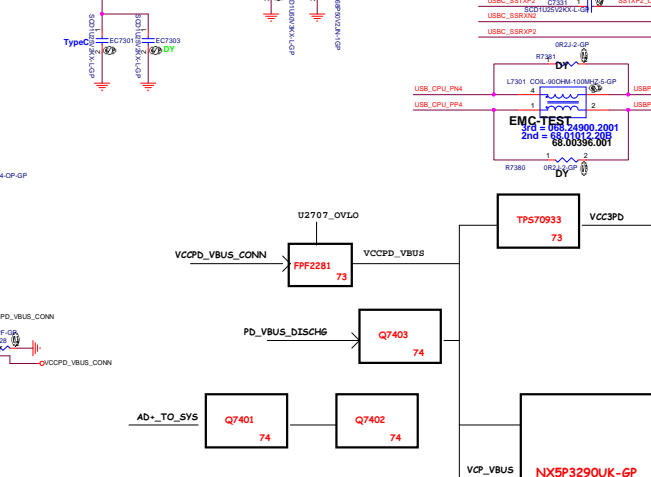
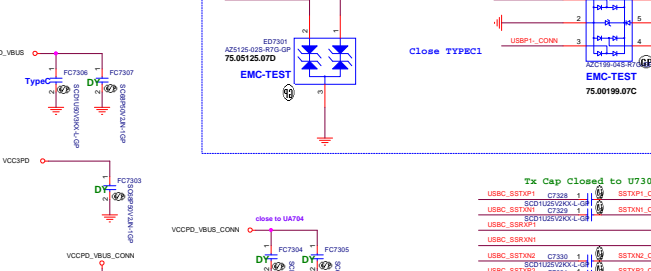
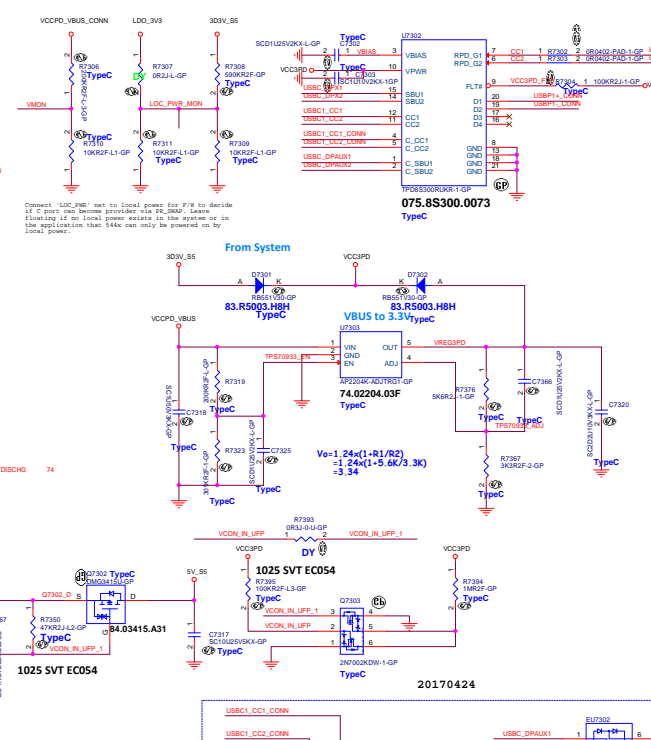
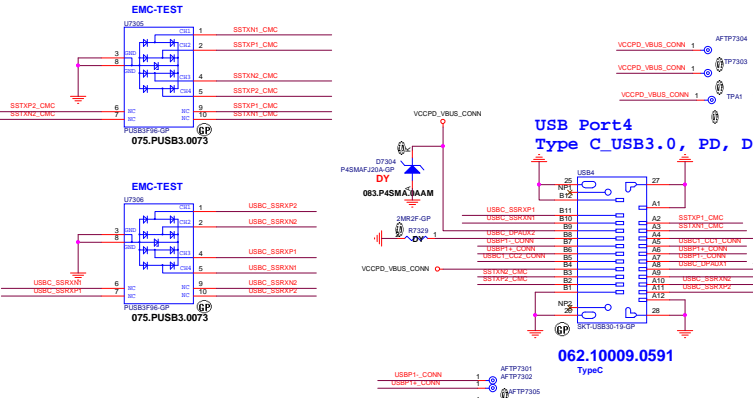


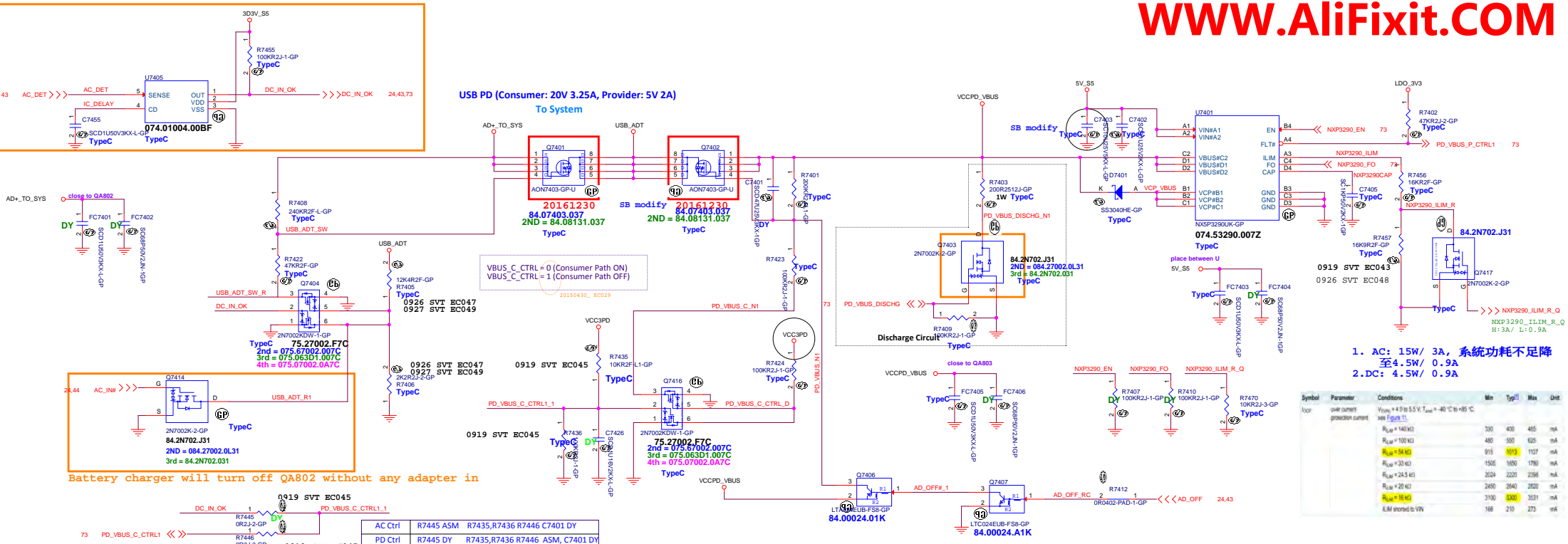
Over-Voltage Lockout (OVLO) Calculation

OVLO can be set externally and override default OVLP by connecting an external resistor-driver to the OVLO pin. Equation (1) can produce the desired trip voltage and resistor values.

$$V_{IN_OVLO} = V_{CCPD_VBUS} \times [1 + R1/R2]$$

Recommended minimum R1 = 1 MΩ.

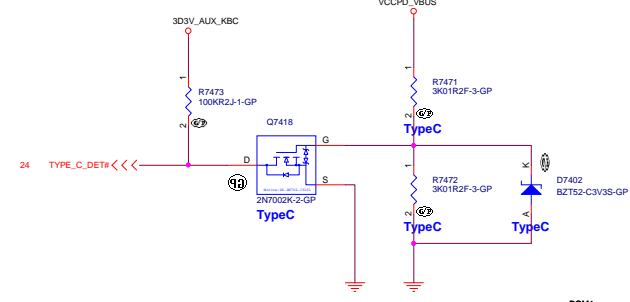




1. AC: 15W / 3A, 系統功耗不足降
至4.5W / 0.9A
2. DC: 4.5W / 0.9A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{load}	over current protection current	V _{IN} = +11.55V, T _{amb} = +40 °C to +85 °C				
R _{DS(on)}	R _{DS(on)}		300	400	405	mΩ
R _{DS(on)}	R _{DS(on)}		400	500	625	mΩ
R _{DS(on)}	R _{DS(on)}		915	931	1107	mΩ
R _{DS(on)}	R _{DS(on)}		1555	1650	1780	mΩ
R _{DS(on)}	R _{DS(on)}		2024	2220	2584	mΩ
R _{DS(on)}	R _{DS(on)}		2450	2640	2820	mΩ
R _{DS(on)}	R _{DS(on)}		3100	3300	3531	mΩ
R _{DS(on)}	R _{DS(on)}		168	210	273	mΩ

19V Power source type	Control Pin				PMOS Location	Status	Remark
	Net name	Status	Net name	Status			
Normal adapter Only	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	Control by DC_IN_OK
					Q7402	OFF	Control by PD_VBUS_C_CTRL1
					PU4302	ON	Control by DC_IN_OK or ACAV_IN
Type-C adapter Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	Low	PU4412	OFF	Control by BGATE
					Q7401	ON	
					Q7402	ON	
Normal adapter + Type-C	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	PU4302	OFF	
					Q7401	OFF	
					Q7402	OFF	
Battery Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	High	PU4412	OFF	
					Q7401	OFF	
					Q7402	OFF	
				PU4302	OFF		
				PU4412	ON	Battery to 19V_DCBATOUT	



BOM1

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Size: Document Name: **Unicorn LV530_KBL_MB14** Rev: SA

Customer: **Unicorn LV530_KBL_MB14**

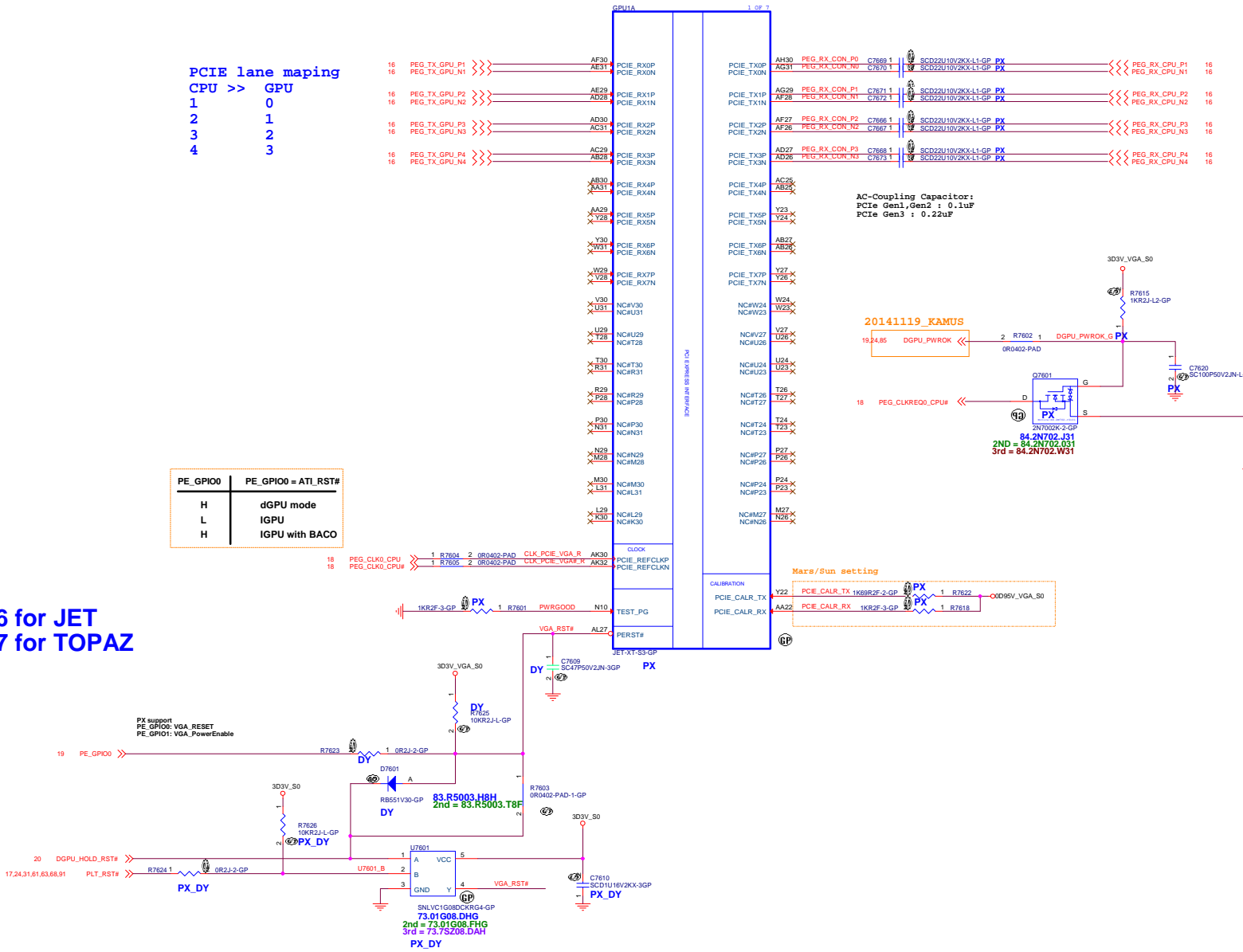
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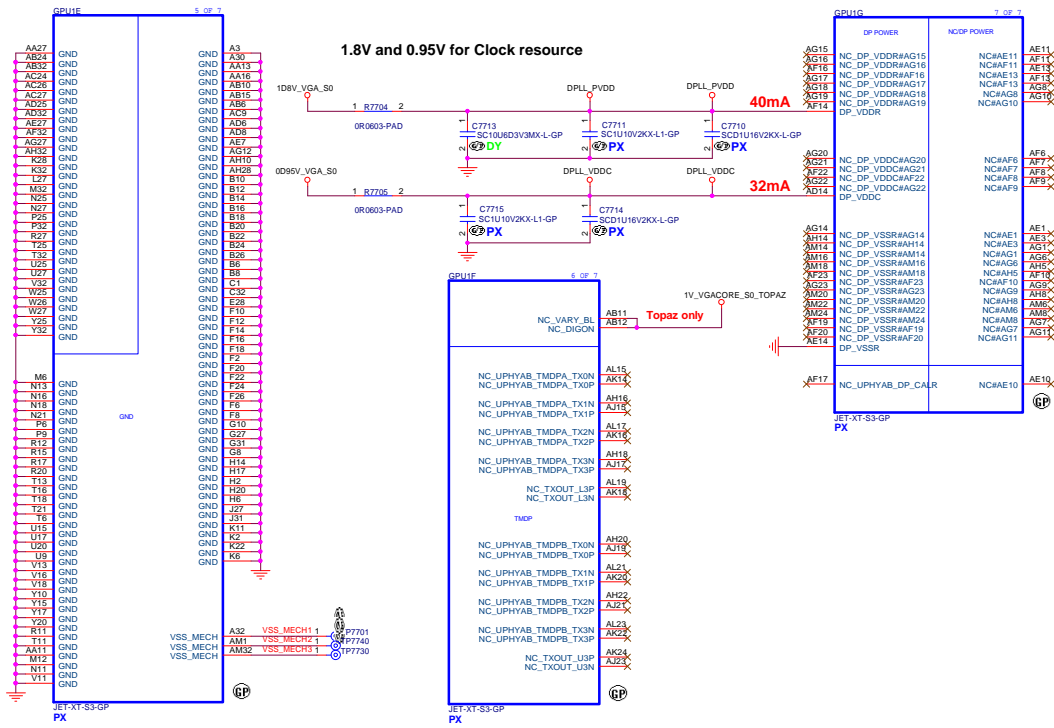
PCIE lane mapping
CPU >> GPU

1	0
2	1
3	2
4	3

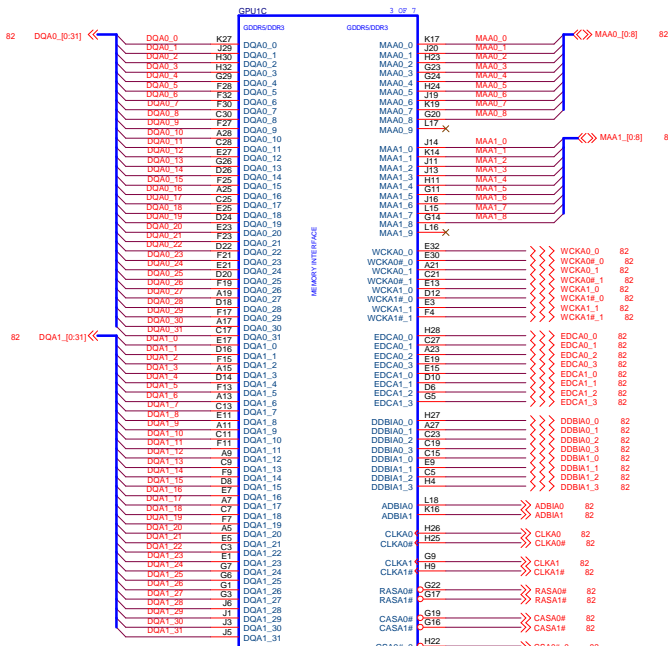
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H	dGPU mode
L	IGPU
H	IGPU with BACO

R16 for JET
R17 for TOPAZ

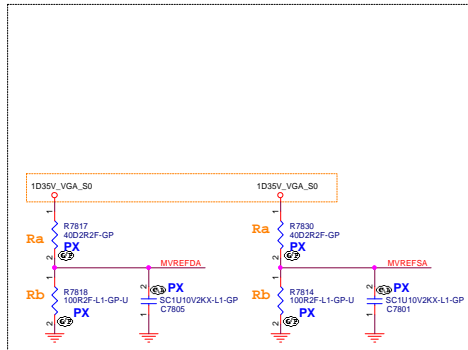




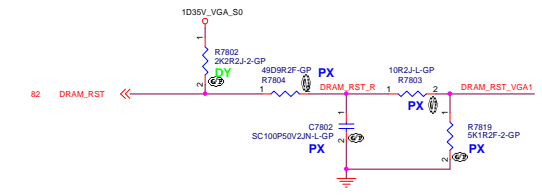
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Size: A2	Document Number: Unicorn_LV530_KBL_MB14	Rev: SA	
Date: Friday, December 15, 2017	Sheet: 77	of: 106	



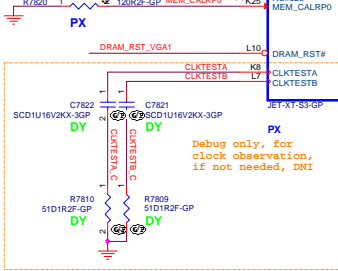
Please MVREF drivers and Caps close to ASIC

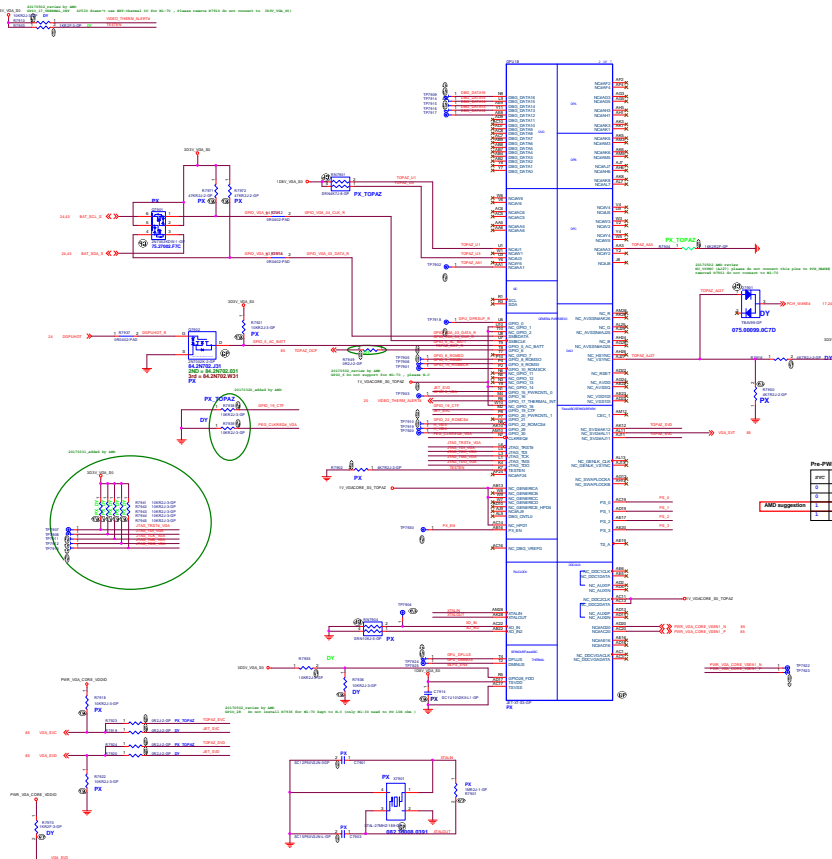


Place all these components very close to GPU (within 25mm) and keep all components close to each other. This basic topology should be used for DRAM_RST for DDR3/GDDR5



Jet Setting





PS0 - PS3 Setting

Cap Value (pF)	Size (S-4)	Part No.	Part No.	Part No.
82	01	8200	2000	801
15	10	6800	6800	6811
NC	11	4330	4330	100
		2262	2262	101
		4750	4750	111

Note: 8202 70% moisture and required.

Board Configs (S-1)

BR	S	4	3	2	1
PS0	1	1	0	0	1
PS2	1	1	0	0	1
PS3	1	1	0	0	1

AMD suggest Aperture Size = 256MB

PS1[1]-0 = K8E2Z only PCIe Gen3 is supported

PS3[3]-1 = 10K_ID setting, need decide for AMD 1000

20170331
Reference below table

Board Configs (2.0)

Pull High	Pull Low	Lenovo PN	Wistron PN	Vendor PN
0	0	NC	4.75Kohm	
0	0	1	8.49K	2K
0	1	0	4.32K	2K
0	1	1	4.32K	4.32K
1	0	0	3.24K	5.22K
1	1	0	3.4K	90K
1	1	1	4750	NC

Vendor PN: Hynix 256M*32 GDDR5.H5GC8H24MUR-R0C 8Gb, Samsung 256M*32 K4G80325FB-HC28 8Gb 7Gbps GDDR5, Micron MT51J256M32HF-70A 8Gb 7Gbps GDDR5

Pin-FUNCTION METAL VIO CODES

Pin	Func	Output	VolRange
1	PS0	1	1.1
2	PS1	1	1.1
3	PS2	1	1.1
4	PS3	1	1.1

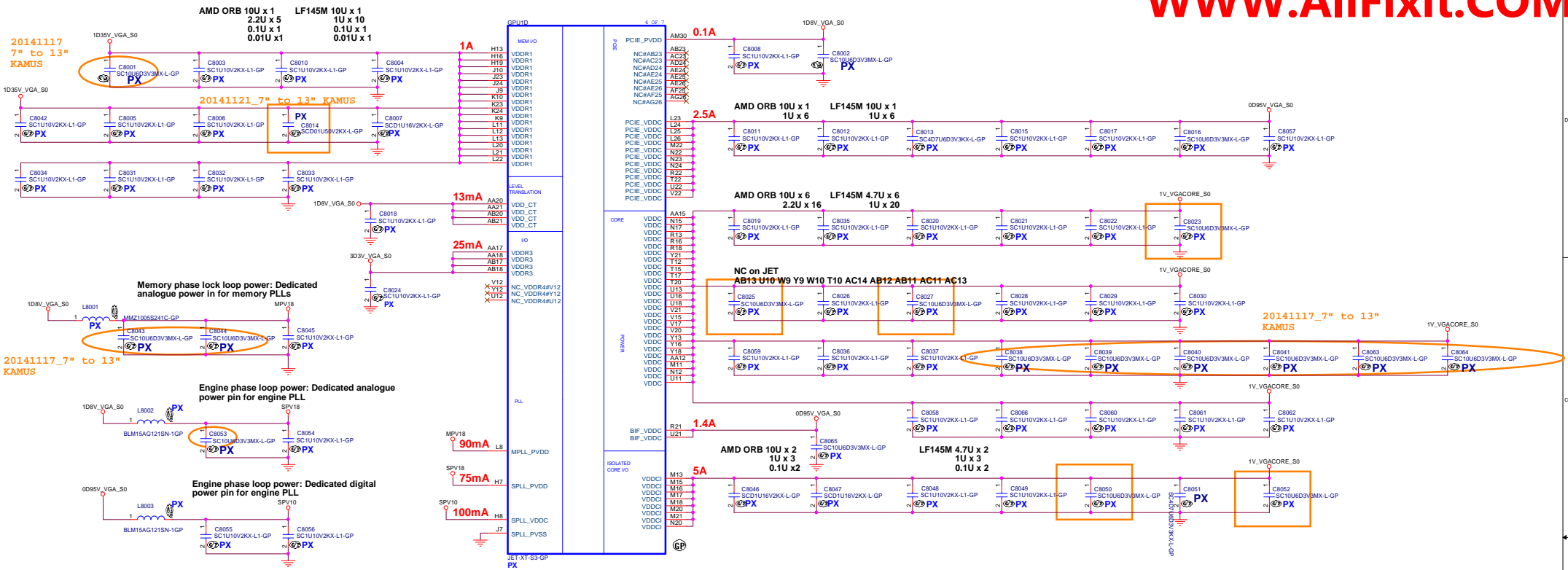
AMD suggestion

CPU Side

GPIOx	GPIOxx
PS0	0
PS1	0
PS2	0
PS3	1

Pin Name	INT	TOTAL
PS0	INT	TOTAL
PS1	INT	TOTAL
PS2	INT	TOTAL
PS3	INT	TOTAL
PS4	INT	TOTAL
PS5	INT	TOTAL
PS6	INT	TOTAL
PS7	INT	TOTAL
PS8	INT	TOTAL
PS9	INT	TOTAL
PS10	INT	TOTAL
PS11	INT	TOTAL
PS12	INT	TOTAL
PS13	INT	TOTAL
PS14	INT	TOTAL
PS15	INT	TOTAL
PS16	INT	TOTAL
PS17	INT	TOTAL
PS18	INT	TOTAL
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PS20	INT	TOTAL
PS21	INT	TOTAL
PS22	INT	TOTAL
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PS94	INT	TOTAL
PS95	INT	TOTAL
PS96	INT	TOTAL
PS97	INT	TOTAL
PS98	INT	TOTAL
PS99	INT	TOTAL
PS100	INT	TOTAL

NC on JET
AB15 U10 W9 Y9 W10 T10 AC10 AB12 AB13 AC11 AC13



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Title GPU VRAM1.2 (1/4)		
Size C	Document Number Unicorn LV530 KBL MB14	Rev SA
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GPU VRAM7,8 (4/4)

Size

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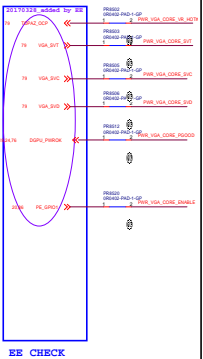
Rev

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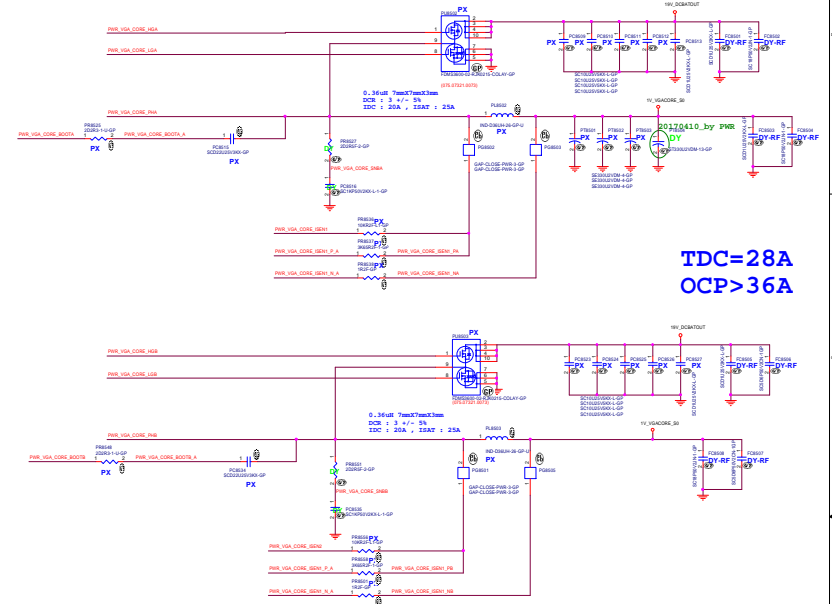
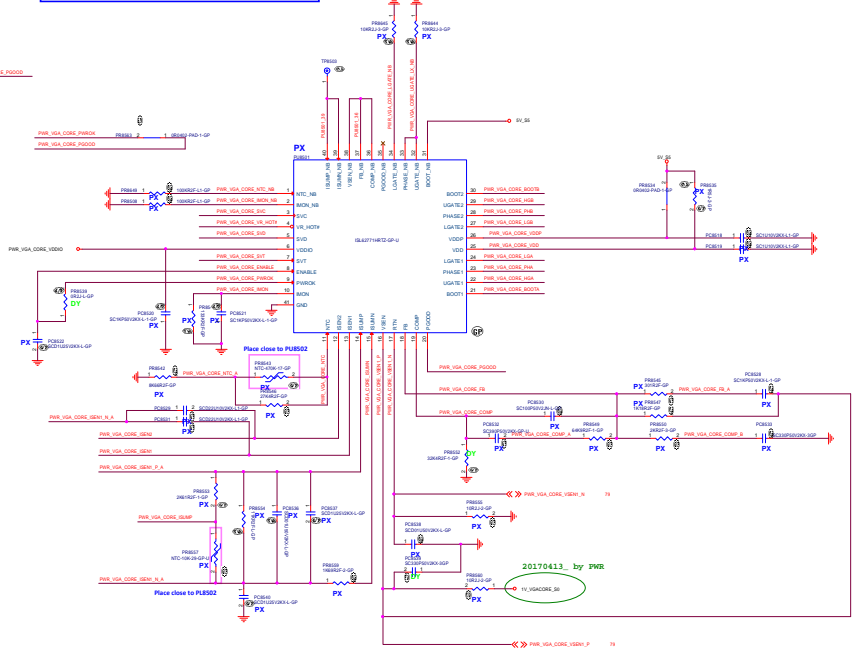
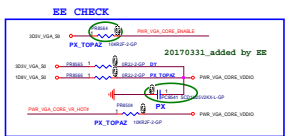
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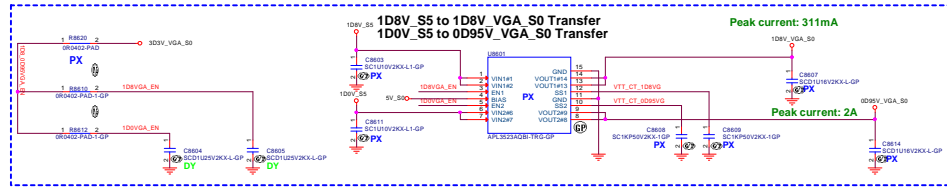
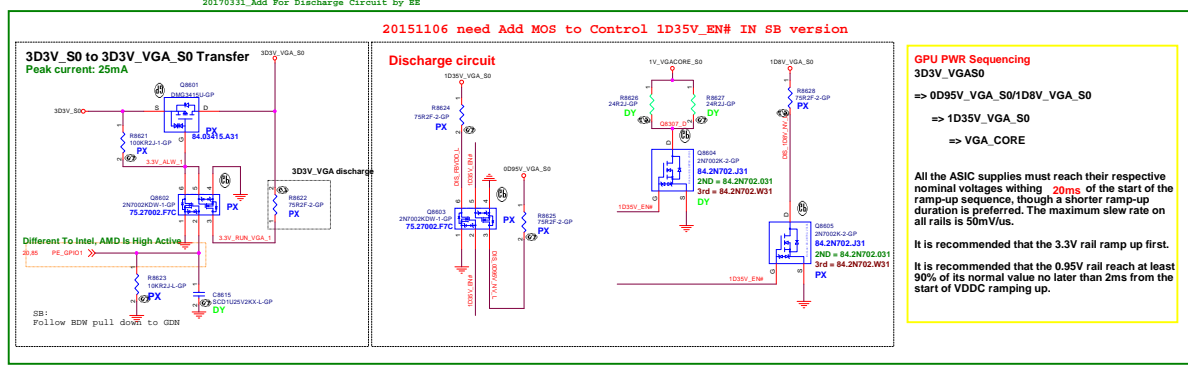
Date: Friday, December 15, 2017

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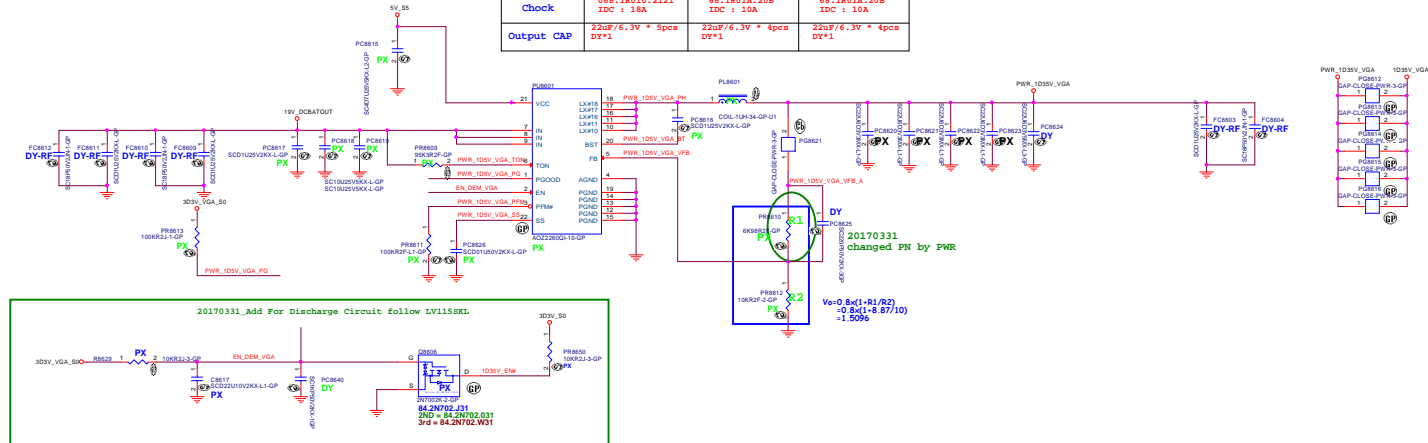
EE CHECK





EE need to confirm 20170208
EE confirm 20170413

IC	AOZ2262 (10A)	AOZ2261 (8A)	AOZ2260 (6A)
COM	668.1801A.2121	66.1801A.208	66.1801A.208
Check	IDC : 1.8A	IDC : 10A	IDC : 10A
Output CAP	22uF/6.3V + 5pcs DY*1	22uF/6.3V + 4pcs DY*1	22uF/6.3V + 4pcs DY*1



<Variant Name>

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Document Number

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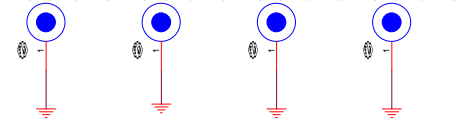
Sheet 88 of 105

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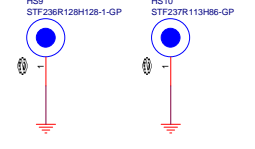
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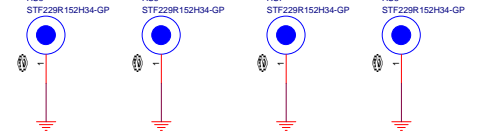
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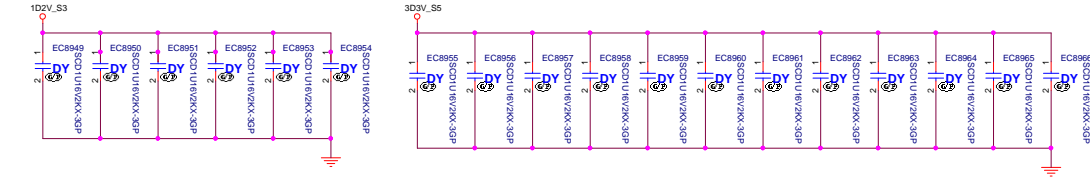
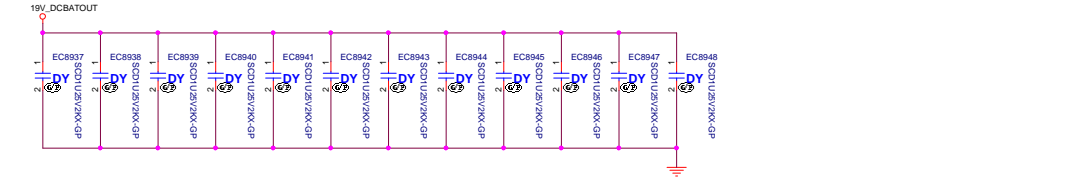
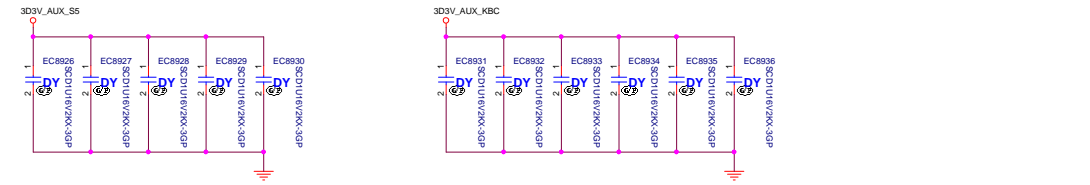
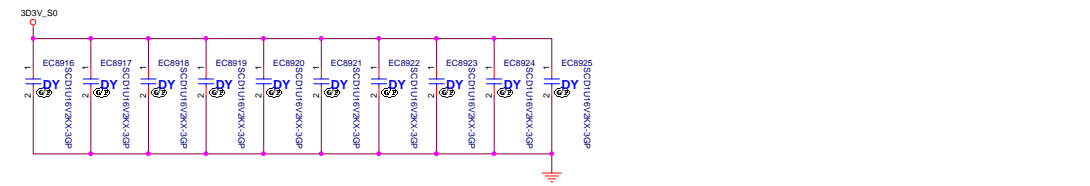
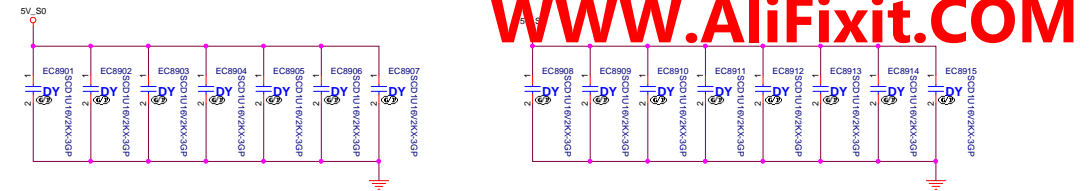
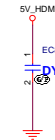
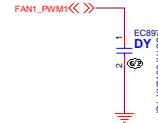
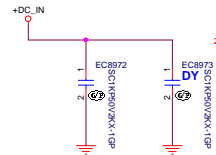
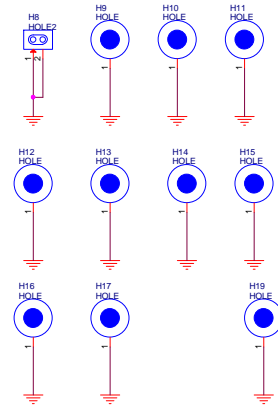
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434.0DB04.0001 434.0DB04.0001 434.0DB04.0001 434.0DB04.0001



ZZ.00PAD.EX1 ZZ.00PAD.EJ1 ZZ.00PAD.FN1



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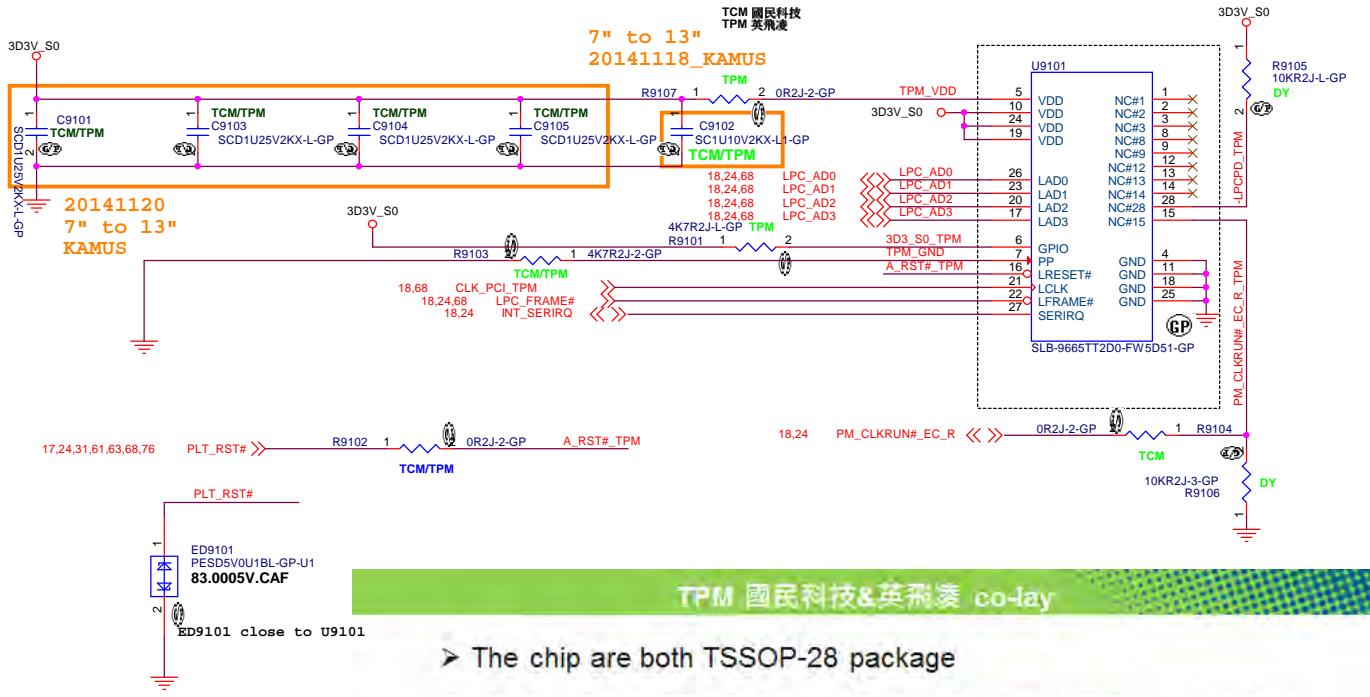
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Unicorn LV530 KBL MB SA

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➤ The chip are both TSSOP-28 package

Pin define	國民	英飛凌	Remark	Pin define	國民	英飛凌	Remark
1	NC	NC		15	CLKRUN#	NC	0ohm
2	NC	NC		16	LRESET#	LRESET#	
3	NC	NC		17	LAD3	LAD3	
4	GND	GND		18	GND	GND	
5	NC	VDD	0ohm	19	VDD	VDD	
6	NC	GPIO	0ohm	20	LAD2	LAD2	
7	NC	PP	0ohm	21	LCLK	LCLK	33ohm for 國民
8	NC	NC		22	LFRAME#	LFRAME#	
9	NC	NC		23	LAD1	LAD1	
10	VDD	VDD		24	VDD	VDD	
11	GND	GND		25	GND	GND	
12	NC	NC		26	LAD0	LAD0	
13	NC	NC		27	SIRQ	SERIRQ	
14	NC	NC		28	LPCLK#	NC	0ohm

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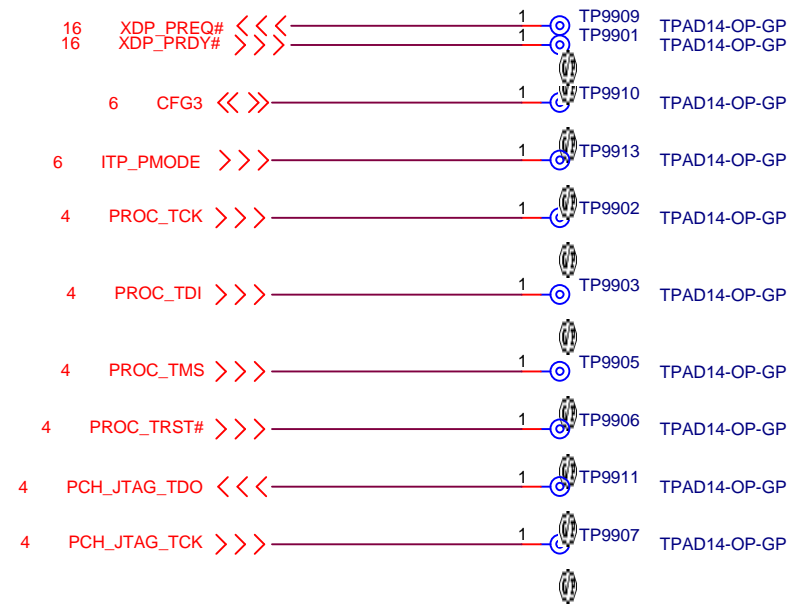
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Title **RESERVED**

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<Variant Name>

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Title **XDP**

Size A4	Document Number Unicorn_LV530_KBL_MB14	Rev SA
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CHANGE HISTORY

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Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)

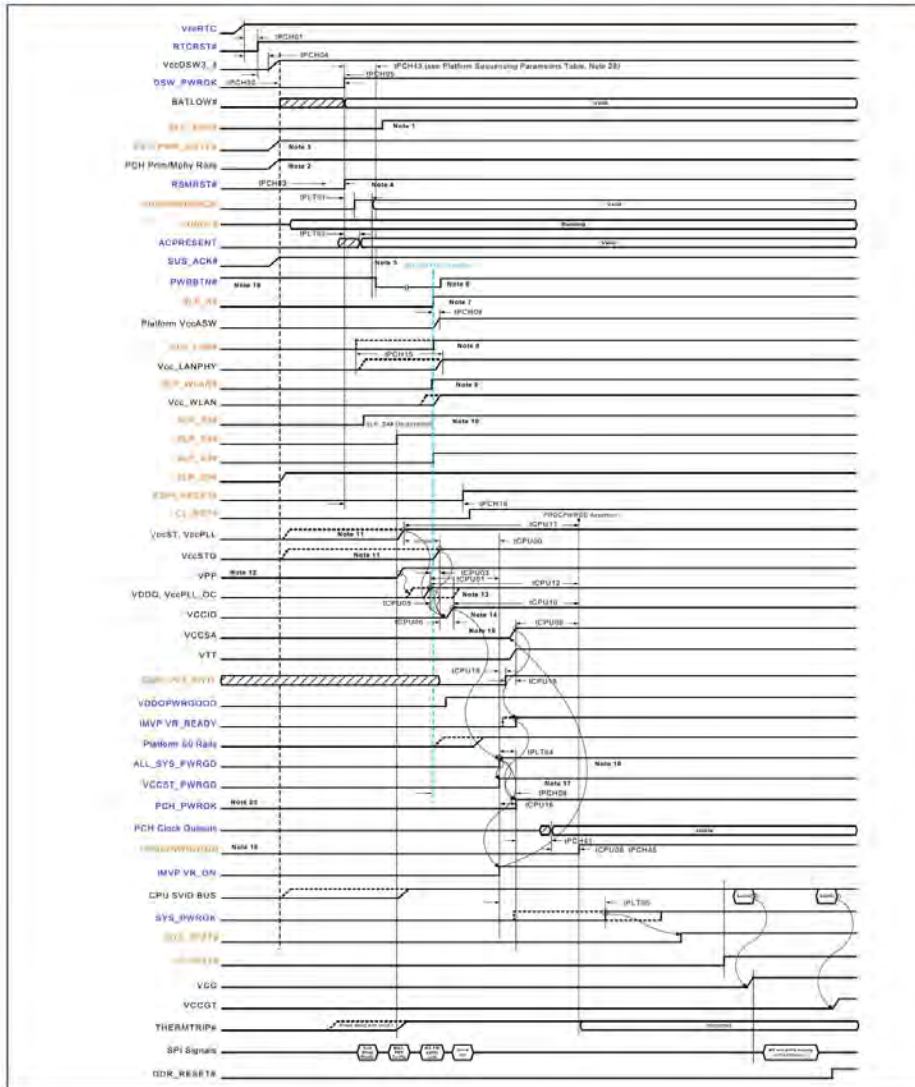


Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 2 of 2)

- Notes:**
1. SLP_SUS# is ignored in Non-DSx systems
 2. Refer Rail-to-Rail Power Sequencing Requirement section for details on PCH prime rail-to-rail power and power down dependencies
 3. EXT_PWR_GATE# has been de-featured. This pin, in native mode, will never be driven low
 4. For a non-DeepSx system DSW_PWROK and RSMRST# go high at the same time (connected on board)
 5. For a non-DeepSx system SUS_ACK# will rise with prime voltage rail powering the VCCPGPPA power pin due to weak internal pull-up.
 6. Minimum duration of PWRBTN# assertion = 16mS. PWRBTN# can assert before or after RSMRST#
 7. On first exit from G3, SLP_A# de-asserts with SLP_S3# de-assertion
 8. High for WoL=1, Low for WoL=0. SLP_LAN# may rise before, but no later than SLP_A#
 9. On first exit from G3, SLP_WLAN# de-asserts with SLP_S3# de-assertion
 10. Delay between SLP_S5#, SLP_S4#, and SLP_S3# exaggerated for drawing purposes. If the system EC is driving these signals in ESPI mode if the, the minimum delay between SLP_S3#, SLP_S4#, and SLP_S5# is not guaranteed
 11. VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization. VCCST, VCCSTG may also remain powered in S4 and S5 for debug purposes. Refer to Chapter 42, "Platform Debug and Test Hooks" for more details. VCCSTG should only ramp up equal to or after VCCST.
 12. Only required with LPDDR3 and DDR4 memory configurations
 13. VDDQ must ramp after VPP on DDR4 and LPDDR3 based systems, thus VDDQ may ramp up after SLP_S3# de-assertion due to VR ramp timing and configuration
 14. VCCIO, VCCSA must ramp after VccSt, VccSTG, and VDDQ have completed their ramps. If VCCSTG and VCCIO supplies are merged together as a single supply, VCCSA must ramp after VccSt, VccSTG/VCCIO, and VDDQ have completed their ramps
 15. IMVP_VR_ON is recommended to be triggered by ALL_SYS_PWRGD in order to help minimize boot latency.
 16. ALL_SYS_PWRGD is assumed to logically AND together the pwrgood signals for the major system power rails
 17. VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it. It is recommended that both VCCST_PWRGD and PCH_PWROK include ALL_SYS_PWRGD in their generation. This ensures during failure events, both signals de-assert at the same time
 18. PROCPWRGD is used only for power sequence debug and is not required to be connected to anything on the platform.
 19. When "Power Button" is the trigger for wake or sleep event for the system
 20. The Platform should ensure that PCH_PWROK does not glitch when RSMRST# is de-asserted

- Additional Notes:**
- The state of the SLP_A# and SUSPWRDNACK signals are used by the EC to determine if PCH requires the suspend-well to stay powered.
- SUSPWRDNACK
 - Platform not supporting M3 - EC must keep SUS Rails powered ON if: SUSPWRDNACK is de-asserted **OR** System state is S3. Else, EC has an option to do whatever it wants with the SUS Rails
 - Platform supporting M3 - EC must keep SUS Rails powered ON if: SUSPWRDNACK is de-asserted **OR** System state is S3 **OR** SLP_A# is de-asserted **OR** it is the first 200mS after SUS Rails power has been applied. Else, EC has an option to do whatever it wants with the SUS Rails
 - Primary rails and Deep Sx Rails should **never** be active while VccRTC rail is inactive.

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