X1757/MLB

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9	9	SOC: PCIE	ref_soc_h13g	05/04/2020
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11	11	SOC: POWER (DDR,SRAM)	ref_soc_h13g	05/04/2020
12	12	SOC: POWER (IO)	ref_soc_h13g	05/04/2020
13	13	SOC: POWER (SOC, CPU, GPU)	ref_soc_h13g	05/04/2020
14	14	SOC: POWER (SRAM)	ref_soc_h13g	05/04/2020
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16	16	SOC: GND	ref_soc_h13g	05/04/2020
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18	18	SOC: DESENSE CAPS	ref_soc_h13g	10/08/2019
19	19	SPI NOR	ref_soc_h13g	05/04/2020
20	21	SOC: Project Support		
21	50	Secure Element	ref_se_ceres	03/29/2020
22	51	BMU Connector, Btn Logic	tga_140	05/31/2019
23	52	PBUS SUPPLY & BATTERY CHARGER	ref_charger_suona	05/02/2020
24	53	BATTERY CHARGER SUPPORT	ref_charger_suona	05/02/2020
25	57	POWER: 3V8 AON (1/2)	ref_vr_iceman	04/20/2020
26	58	POWER: 3V8 AON (2/2)	ref_vr_iceman	04/20/2020
27	59	POWER: 3V8 AON SUPPORT	T585_REF_VR_ICEMAN_0.1	10/01/2019
28	77	PMU: SLAVE INPUT PWR & BUCKS	ref_pmu_sera_simetra	04/28/2020
29	78	PMU: SLAVE LDO	ref_pmu_sera_simetra	04/28/2020
30	79	PMU: SLAVE GPIO & GND	ref_pmu_sera_simetra	04/28/2020
31	80	PMU: Slave extra		
32	81	PMU: MASTER INPUT PWR & BUCKS	ref_pmu_sera_simetra	04/28/2020
33	82	PMU: MASTER BUCKS & GND	ref_pmu_sera_simetra	04/28/2020
34	83	PMU: MASTER LDO & GPIO	ref_pmu_sera_simetra	04/28/2020
35	84	PMU: Master extra		
36	121	Power: LDOs	tga_140	05/31/2019
37	122	POWER: 5V, 3V3 Support		
38	123	POWER: 5V S2	ref_vr_5v_lt8642s	04/20/2020
39	127	POWER: 3V3 S2	ref_vr_3v3_tps62135	01/02/2020
40	128	Power: Load Switches	tga_140	05/31/2019
41	130	I2C: SIO, DISP	eli	10/15/2019
42	131	I2C: ISP, AOP	T668	08/01/2019
43	132	I2C: SMC	T668	08/01/2019
44	135	SENSORS: POWER HIGH SIDE (1/2)	t668	08/27/2019
45	136	SENSORS: POWER HIGH SIDE (2/2)	t668	08/27/2019

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46	138	SENSORS: POWER LOW SIDE (1/2)	t668	08/27/2019
47	140	SENSORS: POWER SUPPORT	t668	08/27/2019
48	141	Sensors: Thermal		
49	144	SENSORS: MOTION	t668	09/27/2019
50	149	RIO Connector	tga_140	05/31/2019
51	150	USB-C: High Speed ATC0	ref_usbc_ace2	04/24/2020
52	151	USB-C: High Speed ATC1	ref_usbc_ace2	04/24/2020
53	152	USB-C: Support 1 ATC01	ref_usbc_ace2	04/24/2020
54	153	USB-C: Support 2 ATC01	ref_usbc_ace2	04/24/2020
55	154	USB-C: Port Controller ATC0	ref_usbc_ace2	04/24/2020
56	155	USB-C: Port Controller ATC1	ref_usbc_ace2	04/24/2020
57	156	USB-C: Connector(s)	ref_usbc_ace2	09/26/2019
58	157	USB-C: HS Level Shifters	ref_usbc_ace2	04/24/2020
59	159	USB-C: Project Specific		
60	200	WIFI/BT: MODULE	ref_wireless_rasputin	04/28/2020
61	201	WIFI/BT: ANTENNA and GND	ref_wireless_rasputin	04/28/2020
62	220	STORAGE: SSD0 S5E <0>	ref_storage_s5e	05/02/2020
63	221	STORAGE: SSD0 S5E <1>	ref_storage_s5e	05/02/2020
64	224	STORAGE: NON OCARINA SUPPORT	ref_storage_non_ocarina	04/28/2020
65	230	STORAGE: SSD Support	T668	08/01/2019
66	231	SECDIS: MIPI MUX	ref_secdis_mipimux	10/07/2019
67	236	eDP Display Connector	tga_140	05/31/2019
68	237	DISPLAY POWER SEQUENCER	ref_panelpwr_bnj	05/02/2020
69	238	BEN: CONTROLLER	ref_blc_ben	11/20/2019
70	239	BEN: KEYBOARD	ref_blc_ben	11/20/2019
71	242	SECDIS: AMR	ref_secdis_amr	10/21/2019
72	243	SECDIS: FPGA	ref_secdis_sak	04/28/2020
73	244	Audio Level Shifters	ref_spkramp_tas5770	11/18/2019
74	246	AUDIO AMPLIFIERS (1/2)	ref_spkramp_tas5770	04/20/2020
75	248	Audio Connectors	tga_140	05/31/2019
76	253	Trackpad Support	ref_ipd_oregano	08/01/2019
77	254	IPD Combined Connector	card_ipd_oregano	08/01/2019
78	260	Power Aliases - 1	tga_140	05/31/2019
79	261	Power Aliases - 2	tga_140	05/31/2019
80	263	Signal Aliases 1		
81	264	Signal Aliases 2		
82	270	DEBUG	tga_140	05/31/2019
83	281	Desense		
84	500	17.2 RULES	eli	10/15/2019
85	501	17.2 PHYSICAL CSETS	eli	10/15/2019
86	502	17.2 SPACING CSETS, ISO	eli	10/15/2019
87	503	17.2 SPACING CSETS, CLASS-CLASS	eli	10/15/2019
88	601	BOM OPTION TABLES	t668	11/01/2019
89	602	BOM GROUPS	t668	11/01/2019
90	610	BOM Alternates		

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A Module Parts

TBT Burnside Bridge

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00561	2	IC,TBT,BBR,SLMN7,PRQ,A1,BGA105	UF000,UF100	CRITICAL	TBT_BB:PRQA1

Ace2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02158	2	IC,CD3217,ACE2,B2,USB PWR SW W/HV,BGA123	UF400,UF500	CRITICAL	ACE2:B2_BGA

eUSB Level Shifter

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-20641	2	IC,PARROT,CD2E224,B0,OTP-6,CSP25	UF700,UF750	CRITICAL	EUSB_LS:B0_OTP6
338S00628	2	IC,PARROT,CD2E226B,B0 LSB1,OTP-6,CSP25	UF700,UF750	CRITICAL	EUSB_LS:B0_LSB1_OTP6

Secure Element

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-19915	1	IC,SN210V,B1,CERES,DEV KY,SWv7,WLCSP81	U5000	CRITICAL	SE:DEV_SW_V7
998-21255	1	IC,SN210V,B1,CERES,DEV,SWv03,WLCSP81	U5000	CRITICAL	SE:DEV_SW_H3
338S00630	1	IC,SN210V,B1,CERES,PROD,VER+MU,WLCSP81	U5000	CRITICAL	SE:PROD_SW_MU

B Programmable Parts

TBT ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	UF260	CRITICAL	TBT_ROM:BLANK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00232	335S00133	TBT_ROM:BLANK	UF260	rdar://problem/50598337

341S01617	1	ROM,TBT/ACE (V31.5) PROTO-1,X1757	UF260	CRITICAL	TBT_ROM:PP0
341S01676	1	ROM,TBT/ACE (V2.45.0.7) PROTO-1,X1757	UF260	CRITICAL	TBT_ROM:PP1

SOC ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-20613	1	IC,SPI SERIAL FLASH,64MBIT,1.8V,XSON8	U1970	CRITICAL	SOC_ROM:BLANK_ORIG
335S00494	1	IC,SPI SERIAL FLASH,64MBIT,1.8V,4X3,SON8	U1970	CRITICAL	SOC_ROM:BLANK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00500	335S00494	SOC_ROM:BLANK	U1970	rdar://problem/59964804

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BOM Configuration

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A BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	SCHEM,PCBF,ALTERNATE,COMMON,CMN_IC,MLB_PROGPARTS,MLB_USBC,MLB_POWER,MLB_WIRELESS,MLB_MECH,MLB_MISC,MLB_BLC,EVT,SECDIS_EXT_CLK,DMIC_CLK_10OHM
MLB_USBC	TBT_BB:PRQA1,ACE2:B2_BGA,UPC_ATCRTMR_INT,UPC_EUSBLS_INT,EUSB_LS:B0_LSB1_OTP6
MLB_PROGPARTS	WFBT_ROM:BLANK,SOC_ROM:BLANK,TBT_ROM:PP1,SE:PROD_SW_MU
MLB_POWER	PBUS_3S,MPMU_IC:B0,SPMU_IC:A1,P3V8AON_IC:A1_R0B0
MLB_WIRELESS	WLBT:ES6_3_M
MLB_MECH	SHLD_CAN_BSB:EVT,SHLD_CAN_ICE:EVT
MLB_MISC	BOARD_ID,SYSDET:FET,BOOT_CONFIG2,LOADISNS
MLB_DEV	DEVELOPMENT,WLBT_DBG,USBC_DBG
MLB_BLC	BLC_BEN_IC:V7,BLC_LEDS_PER_STRING:16,BLC_5V_CAP:4P7_UF,BLC_5V_SERIES:10_OHM,BLC_KBD_BOOST_USED:YES

B Build Specific Groups

BOM GROUP	BOM OPTIONS	
BOARD_ID	BOARDID1,BOARDID2	Pull-ups: 0x0000110
PROTO0	BOARD_REV3,BOARD_REV2,BOARD_REV1,BOARD_REV0	Pull-downs: 0x0000
PROTO1	BOARD_REV3,BOARD_REV2,BOARD_REV1	Pull-downs: 0x0001
EVT	BOARD_REV3,BOARD_REV2,BOARD_REV0	Pull-downs: 0x0002

C DC/DC BOM Groups

BOM GROUP	BOM OPTIONS
DCDC_COMMON	SCHEM,PCBF,COMMON,DCDC_USBC,MLB_POWER,MLB_MECH,MLB_MISC,MLB_BLC,EVT
DCDC_USBC	UPC_ATCRTMR_INT,UPC_EUSBLS_INT

D Reference Design Pack Options

PACK_OPTIONS TO INCLUDE IN NETLIST
USBC_SPI_UPC0
USBC_DEBUG_UPC0
USBC01_VR5V_LOCAL_NO
USBC_LAPTOP
NO_DFR
FTCAM
HAS_LID

PACK_OPTIONS TO INCLUDE IN NETLIST
5V_S2_PBUS-D12
3V3_S2_PBUS-D2
3V8_AON_PBUS-B12
3V8_AON_I2C-DEV
NO_AMR_INTERPOSER_LEFT
NO_AMR_INTERPOSER_RIGHT
PKGS:SMALL_PITCH
ACE2_SS_CAP

PACK_OPTIONS TO INCLUDE IN NETLIST
PROD_SECDIS
JTAG_SECDIS:NO
PROTO_PULLDOWN_SECDIS
80UM_STEN
INTERNAL_DISPLAY
CHGR_40W

PACK_OPTIONS TO INCLUDE IN NETLIST
SUNWAY
WLBT_DBG_CONN
SPKRAMP_A
PORTABLE
SMALL_NOR
SPKRAMP_LVL_SON

PACK_OPTIONS TO INCLUDE IN NETLIST
CHGR_TP
CHGR_TP_BOT
3V8_EXT_DIODE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
685-00339	1	COMMON PARTS,MLB,X1757	CBOM	CRITICAL	CMN_PARTS_BOM
685-00377	1	PARTS,SSDNAND1,MLB,X1757	P1BOM	CRITICAL	PARTS_SSDNAND1
985-01176	1	DEV PARTS,MLB,X1757	DEV1	CRITICAL	DEV_PARTS_BOM
051-05392	1	SCHEM,MLB,X1757	SCHEM	CRITICAL	SCHEM
820-02016	1	PCBF,MLB,X1757	PCBF	CRITICAL	PCBF

A Mounting Holes

998-19374
SH0400
TH-NSP
SL-3.41X2.0-5.91X4.5

998-19374
SH0401
TH-NSP
SL-3.41X2.0-5.91X4.5

998-11113
SH0402
4.6R1.7-NSP

998-11114
SH0403
4.6X5.2R1.7X2.3-NSP

B Heatsink Mounting Holes

998-6473
SH0410
4P0R3P15-NSP

998-22161
SH0411
TH-NSP
SL-3.65X3.15-4.45X4.0

998-21888
SH0412
4.45R3.6-NSP

998-21888
SH0413
4.45R3.6-NSP

C Antenna Cowling Bosses

860-01273
SH0420
5.25X2.8R-1.4ID-1.81H-SM

D Burnside Bridge Shield Can

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-19070	1	SHIELD CAN,BURNSIDE BRIDGE,X1419	SHLD1	CRITICAL	SHLD_CAN_BSB
806-26240	1	SHIELD CAN,BURNSIDE BRIDGE,X1739	SHLD1	CRITICAL	SHLD_CAN_BSB:EVT

Plated slots for shield can

SH0430
TH-NSP
SL-0.5X1.28-1.25X2.03

SH0431
TH-NSP
SL-0.5X1.28-1.25X2.03

E Sled, Thermal Module

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-25230	2	SLED,SOLDER,X1757	SLD1,SLD2	CRITICAL	

F Inductor Shield Fence

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-27192	1	SHIELD FENCE,ICEMAN,INDUCTORS,X1739	SHLD2	CRITICAL	SHLD_CAN_ICE
806-27475	1	SHIELD,FENCE,INDUCTORS,X1739	SHLD2	CRITICAL	SHLD_CAN_ICE:EVT

Plated slots for shield can

998-1681
SH0440
TH
SL-0.4X1.20

998-1681
SH0441
TH
SL-0.4X1.20

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PD Parts

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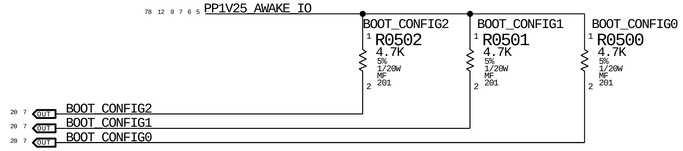
OK2INTEGRATE

BOOT CONFIG ID

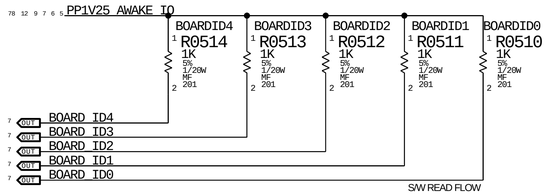


BOOT_CFG[2:0]	MODE
000	SPI1 NOR (12 MHZ)
001	SPI1 NOR (12 MHZ) TESTMODE
010	SPI0 NAND
011	SPI0 NAND TESTMODE
POR ---> 100	SPI1 NOR (40 MHZ)
101	SPI1 NOR (40 MHZ) TESTMODE
110	SPI1 NOR (6 MHZ)
111	SPI1 NOR (6MHZ) TESTMODE

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD ID

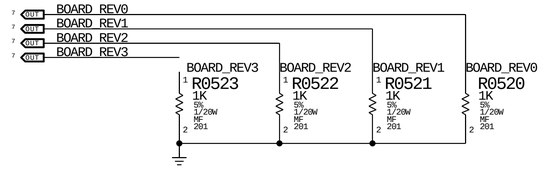


S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD REVISION

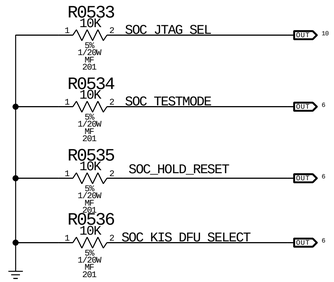
NOTE: STUFFING RESISTOR MEANS 0



board rev should start at 0b0000 and increment each rev.

S/W READ FLOW

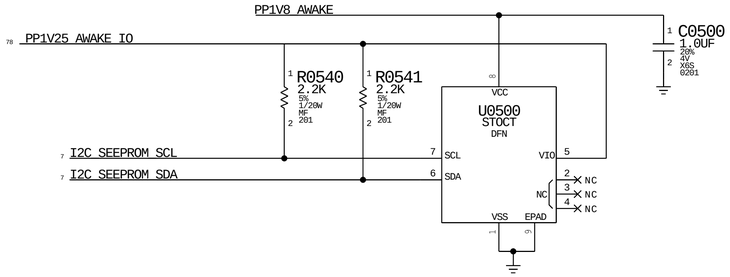
1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ



SEP EEPROM (128-Kbit)

(Write: 0xA2, Read 0xA3)

APN:335S00455



OCELOT I2C pulls

PIN DELAY MAPPING FILE	
REFERENCE DESIGNATOR	PIN DELAY CSV FILE NAME
U0600	TGA_PINDELAY_2020_03_26.csv

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SOC: Support

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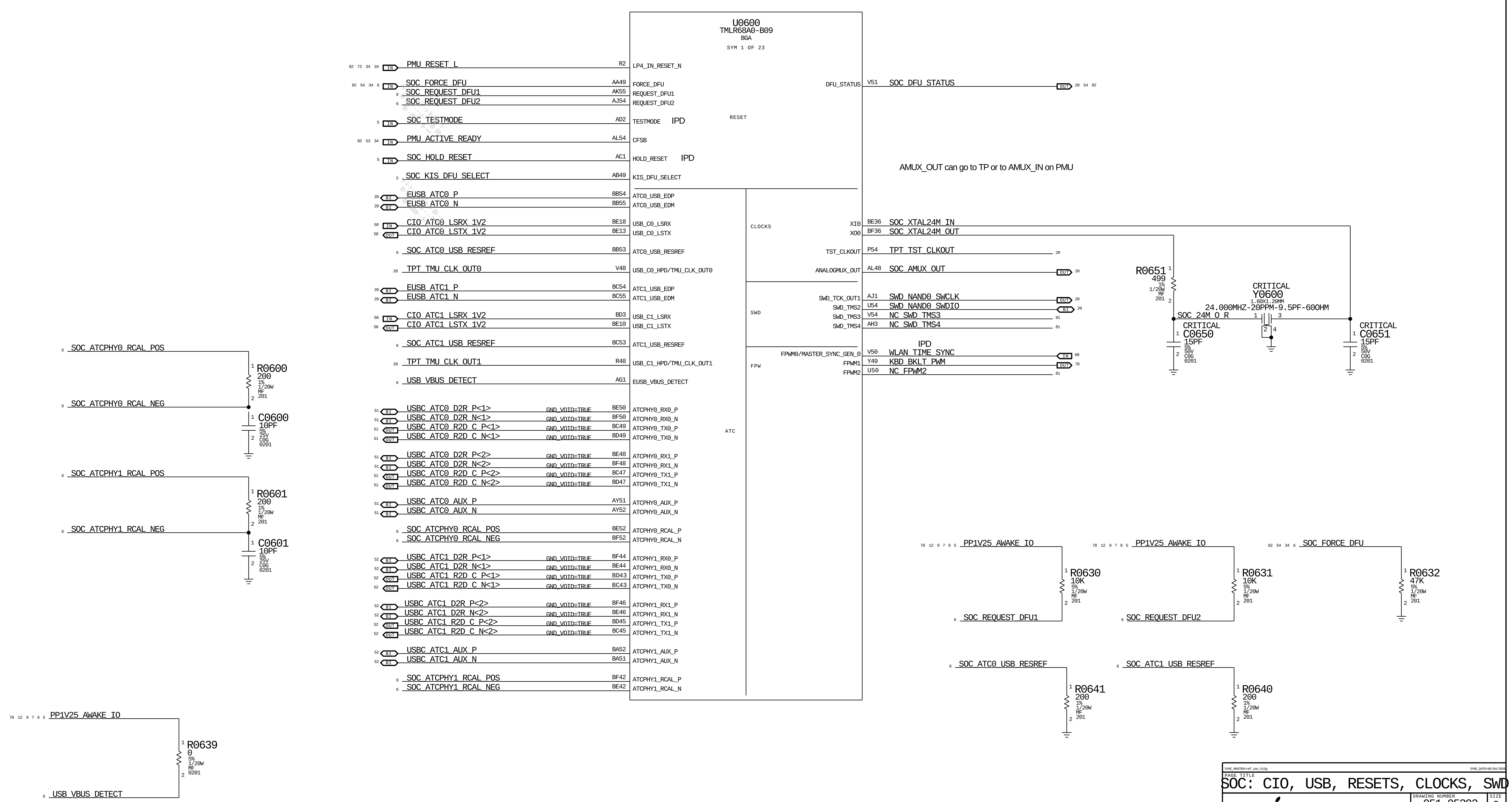
OK2INTEGRATE

SOC: CIO, USB, DRAM, RESETS, CLOCKS, SWD, FPWM



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0590	197S0591		Y0600	EPSON,24MHZ.XTAL
197S0588	197S0591		Y0600	TXC,24MHZ,XTAL

BOM_COST_GROUP=SOC

PAGE TITLE: SOC: CIO, USB, RESETS, CLOCKS, SWD

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OK2INTEGRATE

all signals are 1.2 unless otherwise specified.
all signals on this page reference PP1V2_AWAKE_GRP if they are 1.2V
if they are 1.8V they reference PP1V8_AWAKE_GRP

SOC: I/Os

U0600
TMLR68A0-B09
BGA
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TDM_SPKRAMP_L_BCLK_R	AK4	I2S0_BCLK						
TDM_SPKRAMP_L_D2R	AJ3	I2S0_DIN	IPD					
TDM_SPKRAMP_L_R2D_R	AJ5	I2S0_DOUT						
TDM_SPKRAMP_L_FSYNC_R	AJ4	I2S0_LRCK						
NC_SOC_I2S0_MCK	AK3	I2S0_MCK						
TDM_SPKRAMP_R_BCLK_R	AG3	I2S1_BCLK						
TDM_SPKRAMP_R_D2R	AF3	I2S1_DIN	IPD					
TDM_SPKRAMP_R_R2D_R	AG4	I2S1_DOUT						
TDM_SPKRAMP_R_FSYNC_R	AF2	I2S1_LRCK		I2S	SPI			
NC_SOC_I2S1_MCK	AG2	I2S1_MCK						
TDM_CODEC_BCLK_R	AK5	I2S2_BCLK						
TDM_CODEC_D2R	AL6	I2S2_DIN	IPD					
TDM_CODEC_R2D_R	AJ7	I2S2_DOUT						
TDM_CODEC_FSYNC_R	AM4	I2S2_LRCK						
NC_SOC_I2S2_MCK	AK6	I2S2_MCK						
NC_I2S3_BCLK	AH6	I2S3_BCLK						
NC_I2S3_D2R	AH4	I2S3_DIN						
NC_I2S3_R2D	AG5	I2S3_DOUT						
NC_I2S3_LRCLK	AJ6	I2S3_LRCK						
NC_I2S3_MCLK	AF5	I2S3_MCK						
I2C_UPC_SCL	W52	I2C0_SCL						
I2C_UPC_SDA	V52	I2C0_SDA						
I2C_SPKRAMP_L_SCL	AA48	I2C1_SCL						
I2C_SPKRAMP_L_SDA	Y48	I2C1_SDA			SEP			
NC_I2C_CODEC_SCL	AB50	I2C2_SCL		I2C				
NC_I2C_CODEC_SDA	Y50	I2C2_SDA						
I2C_SPKRAMP_R_CODEC_SCL	AF6	I2C3_SCL						
I2C_SPKRAMP_R_CODEC_SDA	AE6	I2C3_SDA						
NC_I2C_DFR_SCL	AF50	I2C4_SCL						
NC_I2C_DFR_SDA	AG49	I2C4_SDA						
NC_SPMI2_CLK	AK7	AP_SPMI2_SCLK		SPMI				
NC_SPMI2_DATA	AL7	AP_SPMI2_SDATA						

SPI0_MISO	AL4	BOOT_CONFIG2						
SPI0_MOSI	AK2	BOOT_CONFIG1						
SPI0_SCLK	AK1	BOOT_CONFIG0						
SPI1_MISO	AD4	SPI_SOCROM_MISO						
SPI1_MOSI	AE4	SPI_SOCROM_MOSI_R						
SPI1_SCLK	AF4	SPI_SOCROM_CLK_R						
SPI1_SSIN	AE3	SPI_SOCROM_CS_L						
SPI2_MISO	AF53	SPI_1V8_TOUCHID_MISO						
SPI2_MOSI	AF54	SPI_1V8_TOUCHID_MOSI_R						
SPI2_SCLK	AF55	SPI_1V8_TOUCHID_CLK_R						
SPI2_SSIN	AF52	NC_SOC_SPI2_SSIN						
SPI3_MISO	Y1	SPI_IPD_MISO						
SPI3_MOSI	W1	SPI_IPD_MOSI_R						
SPI3_SCLK	AB1	SPI_IPD_CLK_R						
SPI3_SSIN	AA1	SPI_IPD_CS_L						
SPI4_MISO	AC4	SPI_TCON_MISO						
SPI4_MOSI	AB4	SPI_TCON_MOSI_R						
SPI4_SCLK	AA4	SPI_TCON_CLK_R						
SPI4_SSIN	AB3	SPI_TCON_CS_L						
SGPIO0	AC3	DBL_CLICK_DET						
SGPIO1	AC2	DISABLE_STROBE						
SI2C0_SCL	Y5	I2C_SEEPROM_SCL						
SI2C0_SDA	Y4	I2C_SEEPROM_SDA						
SSPI0_MISO	AC5	FTCAM_DISABLE_L						
SSPI0_MOSI	AD5	NC_SSPI0_MOSI						
SSPI0_SCLK	AD6	DMIC_DISABLE_L						
SOCHOT1	AK52	SOC_SOCHOT_L		THROTTLE	IPU FOR ALL THROTTLE_TRIGGER			
THROTTLE_TRIGGER0/MTR_ADC_DOUT	AK53	BUCK1_THERMAL_THROTTLE_L						
THROTTLE_TRIGGER1/MTR_ADC_CLKOUT	AL53	BUCK0_THERMAL_THROTTLE_L						
THROTTLE_TRIGGER2/PLL_DIGOBS_0	AJ55	NC_SOC_TRIGGER2						
THROTTLE_TRIGGER3/PLL_DIGOBS_1	AJ53	PMU_VDDHI_UVWARN_L						
THROTTLE_TRIGGER4	AJ49	PMU_VDDMAIN_UVWARN_L						

1.8V IO

PORTABLES SHOULD NC TRIGGER2

PP1V25_AWAKE_IO
R0790 47K 5% 1/20W MF 201
SOC_SOCHOT_L

U0600
TMLR68A0-B09
BGA
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UPC_I2C_INT_L	AJ51	GPIO[0]	IPU					
NC_SOC_GPIO01	AA50	GPIO[1]						
SPKR_ID0	V53	GPIO[2]	IPU					
SPKR_ID1	U53	GPIO[3]	IPU					
SPKRAMP_RESET_L	T53	GPIO[4]						
SPKRAMP_INT_L	W53	GPIO[5]	IPU		IPD			
CODEC_INT_L	W50	GPIO[6]	IPU		IPD			
SWD_UPC_SWCLK	U52	GPIO[7]						
GPU_CFG_L	AC48	GPIO[8]			IPU			
NC_SOC_GPIO09	R53	GPIO[9]						
NC_SOC_GPIO10	R52	GPIO[10]			IPU			
BOARD_REV0	N55	GPIO[11]						
BOARD_REV1	AH54	GPIO[12]						
BOARD_REV2	Y52	GPIO[13]						
BOARD_REV3	AA51	GPIO[14]						
NC_SOC_GPIO15	R54	GPIO[15]		GPIO	UART			
NC_SOC_GPIO16	AC50	GPIO[16]						
SWD_UPC_SWDIO0	U51	GPIO[17]						
NC_SWD_UPC_SWDIO1	AK50	GPIO[18]						
NC_DFR_TOUCH_INT_L	T52	GPIO[19]						
IPD_SPI_EN	V49	GPIO[20]						
TOUCHID_INT	AJ52	GPIO[21]	IPU					
TOUCHID_PWR_EN	AJ50	GPIO[22]						
UPC_FORCE_PWR	AC49	GPIO[23]						
NC_DFR_PWR_EN	R51	GPIO[24]						
NC_SPI_DFR_CS_L	AL49	GPIO[25]						
NC_ENET_SYNC_1588	AF49	GPIO[26]						
BOARD_ID0	W49	BOARD_ID0/SOC_DEBUG1		BOARD ID	NAND			
BOARD_ID1	R55	BOARD_ID1/SOC_DEBUG2						
BOARD_ID2	T55	BOARD_ID2/SOC_DEBUG3						
BOARD_ID3	V55	BOARD_ID3/SPI0_SSIN						
BOARD_ID4	U55	BOARD_ID4						

UART0_RXD	AB53	UART_DEBUGPRT_D2R						
UART0_TXD	AC53	UART_DEBUGPRT_R2D						
UART1_CTSN	AC54	NC_DFR_1V8_TOUCH_RESET_L						
UART1_RTSN	AA53	NC_DFR_1V8_DISP_RESET_L						
UART1_RXD	AA54	NC_DFR_1V8_DISP_INT						
UART1_TXD	AC55	BT_TIME_SYNC_1V8						
UART2_CTSN	W55	UART_WLAN_D2R_CTS_L						
UART2_RTSN	Y54	UART_WLAN_R2D_RTS_L						
UART2_RXD	Y53	UART_WLAN_D2R						
UART2_TXD	Y55	UART_WLAN_R2D						
UART3_CTSN	AC51	NC_UART3_D2R_CTS_L						
UART3_RTSN	AC52	NC_UART3_R2D_RTS_L						
UART3_RXD	AF48	NC_UART3_D2R						
UART3_TXD	AB52	NC_UART3_R2D						
UART4_CTSN	AJ48	NC_UART4_D2R_CTS_L						
UART4_RTSN	AK48	NC_UART4_R2D_RTS_L						
UART4_RXD	AL52	NC_UART4_D2R						
UART4_TXD	AL50	NC_UART4_R2D						
UART6_RXD	AF51	UART_TCON_D2R						
UART6_TXD	AG50	NC_UART_TCON_R2D						
UART7_RXD	AM2	NC_UART7_RXD						
UART7_TXD	AJ2	NC_UART7_TXD						
NAND_SYS_CLK0	AG52	NAND0_CLK24M_0_R						
NAND_SYS_CLK1	AH53	NAND0_CLK24M_1_R						
SSD_BFH	AH51	NAND_BFH						
SSD_RESETN	AG53	NAND0_RESET_L						

1.8V IO

Use UART2 if your wireless module is 1.2V IO

1.8V IO R2D is for desktop only

NOSTUFF R0791 47K 5% 1/20W MF 201
NAND0_RESET_L

UPC_FORCE_PWR will likely be removed in the future

TOUCHID_PWR_EN gets pulled up to S2 on TOUCHID page
This is OK because the GPIO is failsafe

PD needed on DFR PAGE

BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE
SOC: AP I/Os

Apple Inc.

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SHEET 7 OF 92
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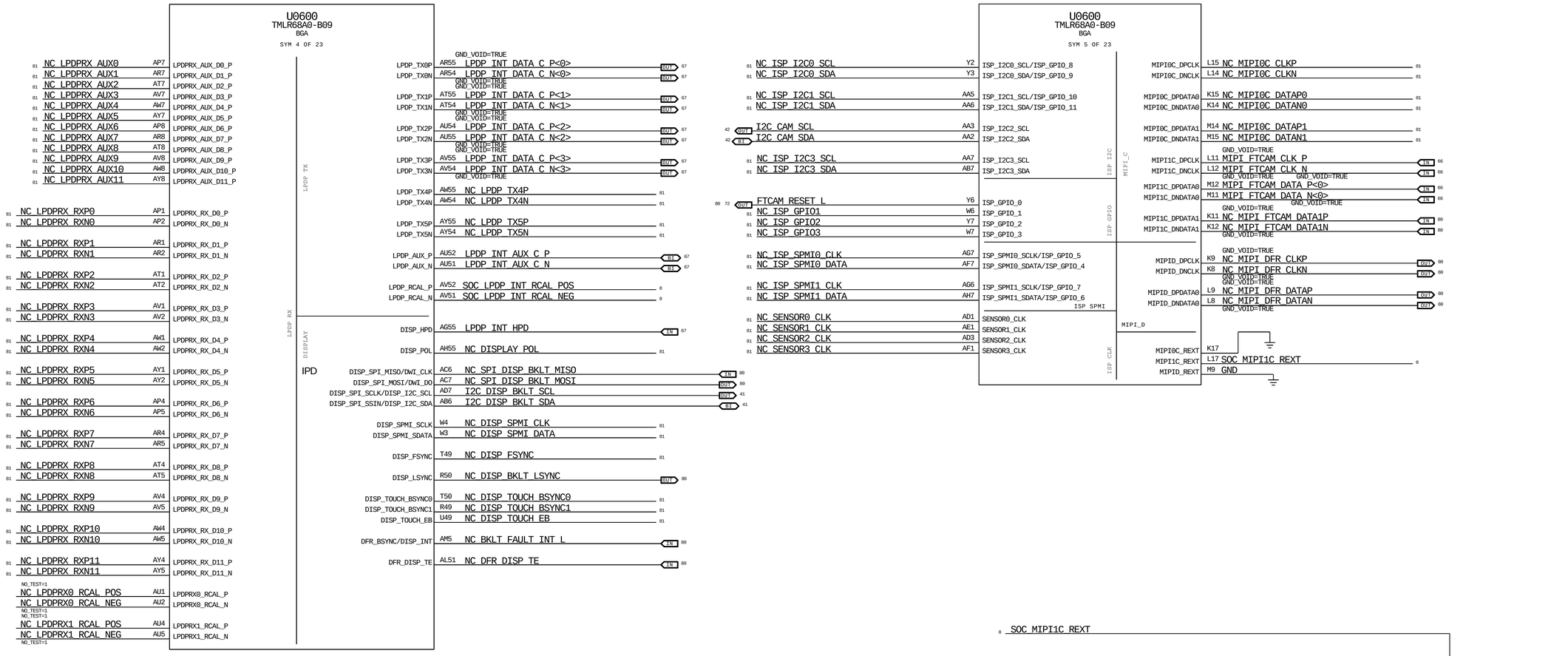
OK2INTEGRATE

SOC: LPDP & MIPI



BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g	SYNC_DATE=05/04/2020
PAGE TITLE	SOC: LPDP & MIPI
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OK2INTEGRATE

SOC: PCIE

PER PCISIG SPEC, AC COUPLING CAPS SHOULD BE BETWEEN
75 NF AND 265 NF FOR GEN1/2 AND BETWEEN
176 NF AND 265 NF FOR GEN 3/4

R0970 IS NEEDED DUE TO RDAR://53793006

78 12 7 6 5 PP1V25_AWAKE_IO

R0930 47K 5% 1/20W MF 201
R0940 47K 5% 1/20W MF 201
R0950 47K 5% 1/20W MF 201
R0970 47K 5% 1/20W MF 201

65 9 NAND0_CLKREQ1_L
61 60 9 WLBT_CLKREQ_L
65 9 NAND0_CLKREQ0_L
9 USBHC_CLKREQ_L

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NAND

62 IN	PCIE_NAND0_D2R_P<0>	BE26	ST_PCIE_RX0_P	PCIE_ST	PCIE_GP
62 IN	PCIE_NAND0_D2R_N<0>	BF26	ST_PCIE_RX0_N		
62 OUT	PCIE_NAND0_R2D_C_P<0>	BC27	ST_PCIE_TX0_P		
62 OUT	PCIE_NAND0_R2D_C_N<0>	BD27	ST_PCIE_TX0_N		
62 OUT	PCIE_CLK100M_NAND0_0_P	BB37	ST_PCIE_REF_CLK0_P		
62 OUT	PCIE_CLK100M_NAND0_0_N	BC37	ST_PCIE_REF_CLK0_N		
65 9 BI	NAND0_CLKREQ0_L	AH50	ST_PCIE_CLKREQ0_N		
62 63 9 OUT	NAND0_PCIE_RESET_L	AH52	ST_PCIE_PERST0_N		
63 IN	PCIE_NAND0_D2R_P<1>	BE28	ST_PCIE_RX1_P	PCIE_ST1	PCIE_GP1
63 IN	PCIE_NAND0_D2R_N<1>	BF28	ST_PCIE_RX1_N		
63 OUT	PCIE_NAND0_R2D_C_P<1>	BC29	ST_PCIE_TX1_P		
63 OUT	PCIE_NAND0_R2D_C_N<1>	BD29	ST_PCIE_TX1_N		
63 OUT	PCIE_CLK100M_NAND0_1_P	BB38	ST_PCIE_REF_CLK1_P		
63 OUT	PCIE_CLK100M_NAND0_1_N	BC38	ST_PCIE_REF_CLK1_N		
65 9 BI	NAND0_CLKREQ1_L	AH49	ST_PCIE_CLKREQ1_N		
81	NC_NAND0_PCIE_RESET1_L	AH48	ST_PCIE_PERST1_N		
9	SOC_ST_PCIE_RCAL_POS	BC24	ST_PCIE_RCAL_P		
9	SOC_ST_PCIE_RCAL_NEG	BB24	ST_PCIE_RCAL_N		
81	NC_PAD_MTR_ANALOG_TEST_POS	AM3	PAD_MTR_ANALOG_TEST_P	MTR	
81	NC_PAD_MTR_ANALOG_TEST_NEG	AL3	PAD_MTR_ANALOG_TEST_N		
81	NC_PAD_MTR_VREF_POS	AL1	PAD_MTR_VREF_P		
81	NC_PAD_MTR_VREF_NEG	AM1	PAD_MTR_VREF_N		

WLAN/BT

GP_PCIE_RX0_P	BE30	PCIE_WLBT_D2R_P	IN	60
GP_PCIE_RX0_N	BF30	PCIE_WLBT_D2R_N	IN	60
GP_PCIE_TX0_P	BC31	PCIE_WLBT_R2D_C_P	OUT	60
GP_PCIE_TX0_N	BD31	PCIE_WLBT_R2D_C_N	OUT	60
GP_PCIE_REF_CLK0_P	BE40	PCIE_CLK100M_WLBT_P	OUT	60
GP_PCIE_REF_CLK0_N	BF40	PCIE_CLK100M_WLBT_N	OUT	60
GP_PCIE_CLKREQ0_N	AB55	WLBT_CLKREQ_L	BI	9 60 61
GP_PCIE_PERST0_N	AA52	WLBT_RESET_L	OUT	9 60 61

USB3 CTLR

GP_PCIE_RX1_P	BE32	NC_PCIE_USBHC_D2RP	IN	80
GP_PCIE_RX1_N	BF32	NC_PCIE_USBHC_D2RN	IN	80
GP_PCIE_TX1_P	BC33	NC_PCIE_USBHC_R2DCP	OUT	80
GP_PCIE_TX1_N	BD33	NC_PCIE_USBHC_R2DCN	OUT	80
GP_PCIE_REF_CLK1_P	BE38	NC_PCIE_CLK100M_USBHCP	OUT	80
GP_PCIE_REF_CLK1_N	BF38	NC_PCIE_CLK100M_USBHCN	OUT	80
GP_PCIE_CLKREQ1_N	AA55	USBHC_CLKREQ_L	BI	9
GP_PCIE_PERST1_N	P55	NC_USBHC_RESET_L	OUT	9 80

ENET/SD

GP_PCIE_RX2_P	BE34	NC_PCIE_ENET_D2RP	IN	80
GP_PCIE_RX2_N	BF34	NC_PCIE_ENET_D2RN	IN	80
GP_PCIE_TX2_P	BC35	NC_PCIE_ENET_R2DCP	OUT	80
GP_PCIE_TX2_N	BD35	NC_PCIE_ENET_R2DCN	OUT	80
GP_PCIE_REF_CLK2_P	BE39	NC_PCIE_CLK100M_ENETP	OUT	80
GP_PCIE_REF_CLK2_N	BF39	NC_PCIE_CLK100M_ENETN	OUT	80
GP_PCIE_CLKREQ2_N	AH1	NC_ENET_CLKREQ_L	BI	9 80
GP_PCIE_PERST2_N	AE7	NC_ENET_RESET_L	OUT	9 80
GP_PCIE_RCAL_P	BC25	SOC_GP_PCIE_RCAL_POS		9
GP_PCIE_RCAL_N	BB25	SOC_GP_PCIE_RCAL_NEG		9

TO BE CHECKED WITH SEG- DO NOT MATCH WITH SILVAL
IS THE PULL-UP VOLTAGE CORRECT?

9 SOC_ST_PCIE_RCAL_POS
R0990 200 1% 1/20W MF 201
9 SOC_ST_PCIE_RCAL_NEG
C0990 10PF 5% 25V C0G 0201

9 SOC_GP_PCIE_RCAL_POS
R0991 200 1% 1/20W MF 201
9 SOC_GP_PCIE_RCAL_NEG
C0991 10PF 5% 25V C0G 0201

63 62 9 NAND0_PCIE_RESET_L
61 60 9 WLBT_RESET_L
R0941 47K 5% 1/20W MF 201
R0951 47K 5% 1/20W MF 201

BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE: SOC: PCIE

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OK2INTEGRATE

AOP, NUB, and SMC GPIO's are referenced to PP1V25_S2_AOP

SOC: AOP

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output if gyro, input for radar

72 IN LID_OPEN MAKE_BASE=TRUE
PACK_OPTION=HAS_LID

I2C0 is ALS for portables

80		NC_AOP_FUNC0	BB18	AOP_FUNC[0]			
81		NC_AOP_FUNC1	BC16	AOP_FUNC[1]			
80		NC_AOP_FUNC2	BC12	AOP_FUNC[2]			
80		NC_AOP_FUNC3	BC13	AOP_FUNC[3]			
80		NC_SPI_R1_CS_L	BA16	AOP_FUNC[4]			
81		NC_AOP_FUNC5	BA13	AOP_FUNC[5]			
49	OUT	SPI_GYRO_CS_L	BA15	AOP_FUNC[6]			
49	IN	GYRO_INT	BD13	AOP_FUNC[7]			
49	IN	GYRO_MOTION_INT	BD16	AOP_FUNC[8]	AOP GPIO		
		LID_OPEN	BA14	AOP_FUNC[9]	IPD		
81		NC_AOP_FUNC10	BB12	AOP_FUNC[10]			
61 60	OUT	WLAN_CONTEXT_A	BD20	AOP_FUNC[11]			
61 60	OUT	WLAN_CONTEXT_B	BA11	AOP_FUNC[12]			
80	IN	NC_ALS_INT_L	BD18	AOP_FUNC[13]			
81		NC_AOP_FUNC14	BA10	AOP_FUNC[14]			
42	OUT	I2C_AOP_ALS_SCL	BC20	AOP_I2C0_SCL			
42	BI	I2C_AOP_ALS_SDA	BB19	AOP_I2C0_SDA	AOP I2C		
42	OUT	NC_I2C_AOP_ENET_SCL	BB16	AOP_I2C1_SCL			
42	BI	NC_I2C_AOP_ENET_SDA	BE15	AOP_I2C1_SDA			
81		NC_PDM_CLK1	BB9	AOP_PDM_IN_CLK1/AOP_I2S1_BCLK			
81		NC_PDM_CLK2	BC9	AOP_PDM_IN_CLK2/AOP_I2S0_MCK			
72	OUT	PDM_DMIC_CLK3	BC6	AOP_PDM_IN_CLK3/AOP_I2S0_LRCK			
72	OUT	PDM_DMIC_CLK4	BD9	AOP_PDM_IN_CLK4/AOP_I2S0_DOUT			
81		NC_PDM_CLK5	BC8	AOP_PDM_IN_CLK5/AOP_I2S0_DIN			
81		NC_PDM_CLK6	BD8	AOP_PDM_IN_CLK6/AOP_I2S0_BCLK	AOP PDM		
81		NC_PDM_DATA1	BE21	AOP_PDM_IN_DATA1/AOP_I2S1_MCK			
81		NC_PDM_DATA2	BE16	AOP_PDM_IN_DATA2/AOP_I2S1_LRCK			
72 IPD	IN	PDM_DMIC_DATA3 CKPLUS_WAIVE=CLK_DATA_CON	BE19	AOP_PDM_IN_DATA3/AOP_I2S1_DOUT/AOP_PDM_IN_CLK7			
72 IPD	IN	PDM_DMIC_DATA4 CKPLUS_WAIVE=CLK_DATA_CON	BD5	AOP_PDM_IN_DATA4/AOP_I2S1_DIN/AOP_PDM_IN_CLK8			
20	IN	SPI_AOP_GYRO_MISO	BF15	AOP_SPI0_MISO			
20	OUT	SPI_AOP_GYRO_MOSI_R	BF14	AOP_SPI0_MOSI	AOP SPI		
20	OUT	SPI_AOP_GYRO_CLK_R	BF17	AOP_SPI0_SCLK			
81		NC_AOP_SPMI0_SCLK	BF18	AOP_SPMI0_SCLK/AOP_UART0_TXD			
81		NC_AOP_SPMI0_SDATA	BF19	AOP_SPMI0_SDATA/AOP_UART0_RXD			
20	OUT	SPMI_SE_CLK_R	BF20	AOP_SPMI1_SCLK/AOP_UART1_TXD	AOP SPMI		
20	BI	SPMI_SE_DATA_R	BF21	AOP_SPMI1_SDATA/AOP_UART1_RXD			
81		NC_AOP_UART2_D2R	BB3	AOP_UART2_RXD			
81		NC_AOP_UART2_R2D	BB4	AOP_UART2_TXD	AOP UART		
34	IN	PMU_CLK32K_SOC	BE6	RT_CLK32768			
			BF10	CFSB_AON	AOP RESET		
82 72 34 6	IN	PMU_RESET_L	BB5	COLD_RESETN			
81		NC_AON_SLEEP1_RESET_L	BB21	AON_SLEEP1_RESETN			
34	OUT	SOC_WDOG	BF12	WDOG			
78 12 10		PP1V25_S2 SOC_DBG_PROBE_VALID	BF6	DBG_PROBE_VALID			
58	BI	EUSB_DBG_P	BF24	DBG_USB_EDP	AOP DEBUG		
58	BI	EUSB_DBG_N	BE24	DBG_USB_EDM			
		SOC_USBDBG_RESREF	BE23	DBG_USB_RESREF			
		NUB_CLK_OUT0	BA17	NC_DFR_TOUCH_CLK32K_RESET_L		OUT	80
		NUB_DOCK_ATTENTION/CTM_TRIGGER	BC15	TPT_SOC_DOCK_ATTENTION			20
		NUB_DOCK_CONNECT	BC17	SOC_DOCK_CONNECT		IN	10 80
		NUB_GPIO_0/AOP_FUNC15/NUB_CLK_OUT1	BD14	NC_BKLT_PWR_ON		OUT	80
		NUB_GPIO_1/AOP_PDM_IN_CLK0	BD15	CODEC_RESET_L		OUT	50
		NUB_GPIO_2/AOP_PDM_IN_DATA0	BD21	SOC_SW_DBG		OUT	82
		NUB_GPIO_3/AOP_LEAP_MADI_IN	BD17	IPD_SPI_INT_L		IN	80
	IPU	NUB_GPIO_4/AOP_LEAP_MADI_OUT	BB13	SMC_FIXTURE_MODE_L		IN	20
		NUB_GPIO_5/AOP_PDM_OUT_CLK0	BD19	CHGR_INT_L		IN	80
		NUB_GPIO_6/AOP_PDM_OUT_DATA0/AOP_FUNC16	BD22	NC_CCG_SMC_I2C_INT_L		IN	80
		NUB_GPIO_7/AOP_FUNC17	BB10	NC_ACDC_ID		IN	80
		NUB_GPIO_8/AOP_FUNC18	BD12	NC_ACDC_BURST_EN_L		OUT	80
NUB GPIO		NUB_GPIO_9/AOP_FUNC19	BD11	NC_SPI_DP2HDMI_HOLD_L		OUT	80
		NUB_GPIO_10/AOP_FUNC20	BC10	NC_HDMI_CEC_AOP_TX		OUT	80
		NUB_GPIO_11/KIS_GPIO0/AOP_FUNC21	BB7	NC_HDMI_CEC_AOP_RX		IN	80
		NUB_GPIO_12/KIS_GPIO1/AOP_FUNC22	BD10	NC_HDMI_HPD_AOP		IN	80
		NUB_SPMI0_SCLK	BB15	SPMI_NUB_MPMU_CLK_R		OUT	20
		NUB_SPMI0_SDATA	BC14	SPMI_NUB_MPMU_DATA_R		BI	20
NUB SPMI		NUB_SPMI1_SCLK	BA12	SPMI_NUB_SPMU_CLK_R		OUT	20
		NUB_SPMI1_SDATA	BC11	SPMI_NUB_SPMU_DATA_R		BI	20
		NUB_SWD_TCK_OUT0	BC18	SWD_NUB_SWCLK		OUT	30 34
		NUB_SWD_TMS0	BC19	SWD_NUB_PMU_SWDIO		BI	30 34
NUB SWD		NUB_SWD_TMS1	BC21	NC_NUB_SWD_TMS1			80
		JTAG_SEL	BE4	SOC_JTAG_SEL		IN	5
	IPU	JTAG_TCK	BF5	SWD_SOC_SWCLK		IN	54
	IPU	JTAG_TDI	BF16	TPT_JTAG_SOC_TDI			20
JTAG		JTAG_TDO	BC1	TPT_JTAG_SOC_TDO			20
	IPU	JTAG_TMS	BB1	SWD_SOC_SWDIO		BI	54
	IPD	JTAG_TRSTN	BF7	TPT_JTAG_SOC_TRST_L			20
		SMC_I2CM0_SCL	BC3	I2C_SMC_PWR_SCL		OUT	43
		SMC_I2CM0_SDA	BC2	I2C_SMC_PWR_SDA		BI	43
		SMC_I2CM1_SCL/SMC_UART1_TXD	BD4	I2C_SMC_UPC_SCL		OUT	43
		SMC_I2CM1_SDA/SMC_UART1_RXD	BB2	I2C_SMC_UPC_SDA		BI	43
		SMC_I2CM2_SCL	BD6	NC_I2C_SMC_SNS1_SCL		OUT	43
SMC I2C		SMC_I2CM2_SDA	BC5	NC_I2C_SMC_SNS1_SDA		BI	43
		SMC_I2CM3_SCL	BC7	I2C_SMC_IPD_SCL		OUT	43
		SMC_I2CM3_SDA	BD7	I2C_SMC_IPD_SDA		BI	43
		SMC_I2CM4_SCL	BE7	NC_I2C_SMC_SNS0_SCL		OUT	43
		SMC_I2CM4_SDA	BF9	NC_I2C_SMC_SNS0_SDA		BI	43
	IPU	SMC_UART0_RXD	BF4	UART_SMC_DEBUGPRT_D2R		IN	54
SMC UART		SMC_UART0_TXD	BF8	UART_SMC_DEBUGPRT_R2D		OUT	54
	IPU	SMC_GPIO0	BF11	UPC_SMC_I2C_INT_L		IN	43
		SMC_GPIO1	BF13	NC_SMC_GPIO1			81
SMC GPIO		SMC_FPWM0	BE12	NC_SMC_FAN_PWM_SMC_SIL_LED_PWM		OUT	80
		SMC_FPWM1	BE9	NC_SMC_FAN_TACH		IN	80

R1083 10K 5% 1/20W MF 201 — PP1V25_S2 — PMU_RESET_L

XW1022 SHORT-14L-0.1MM-SM

R1042 200 1% 1/20W MF 201 — SOC_USBDBG_RESREF

DOC_ATTENTION should be a TP for non dev programs,

SOC_SW_DBG SHOULD GO TO A LED IF POSSIBLE. NEEDS A TEST POINT AT MINIMUM

FIXTURE_MODE_L should be aliased to a TP for non dev programs, The TP is required

80 10 SOC_DOCK_CONNECT

R1066 47K 5% 1/20W MF 201

BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE: SOC: AOP

Apple Inc.

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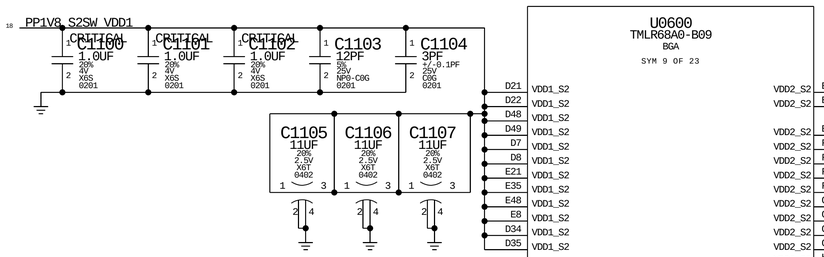
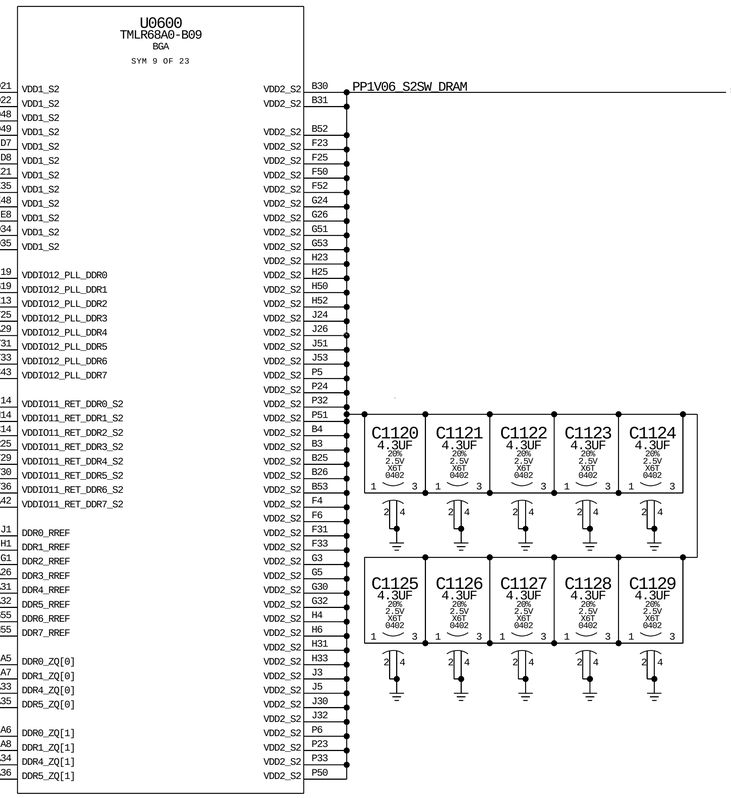
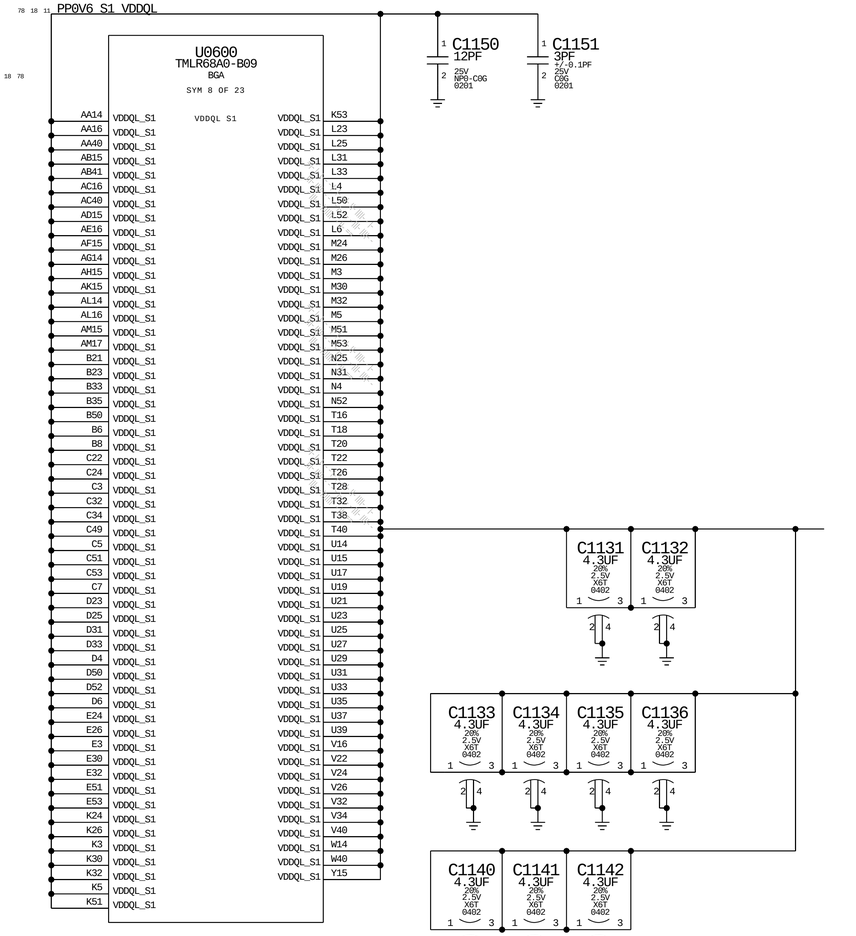
OK2INTEGRATE

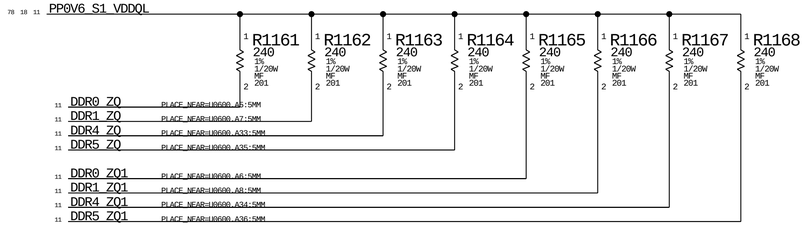
SOC: POWER (DDR,SRAM)

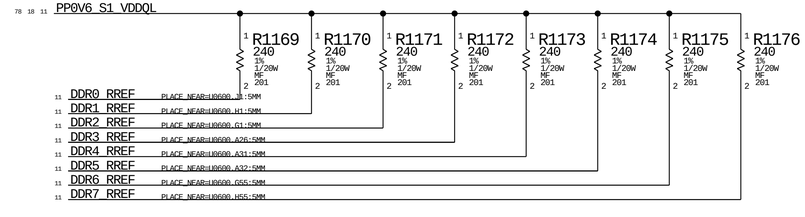
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00139	138S00138		ALL	4.7UF 20% 4V 0201
138S00164	138S00138		ALL	4.7UF 20% 4V 0201











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SYNC_MASTER=ref_soc_h13g/ SYNC_DATE=05/04/2020

PAGE TITLE
SOC: POWER (DDR,SRAM)

Apple Inc.

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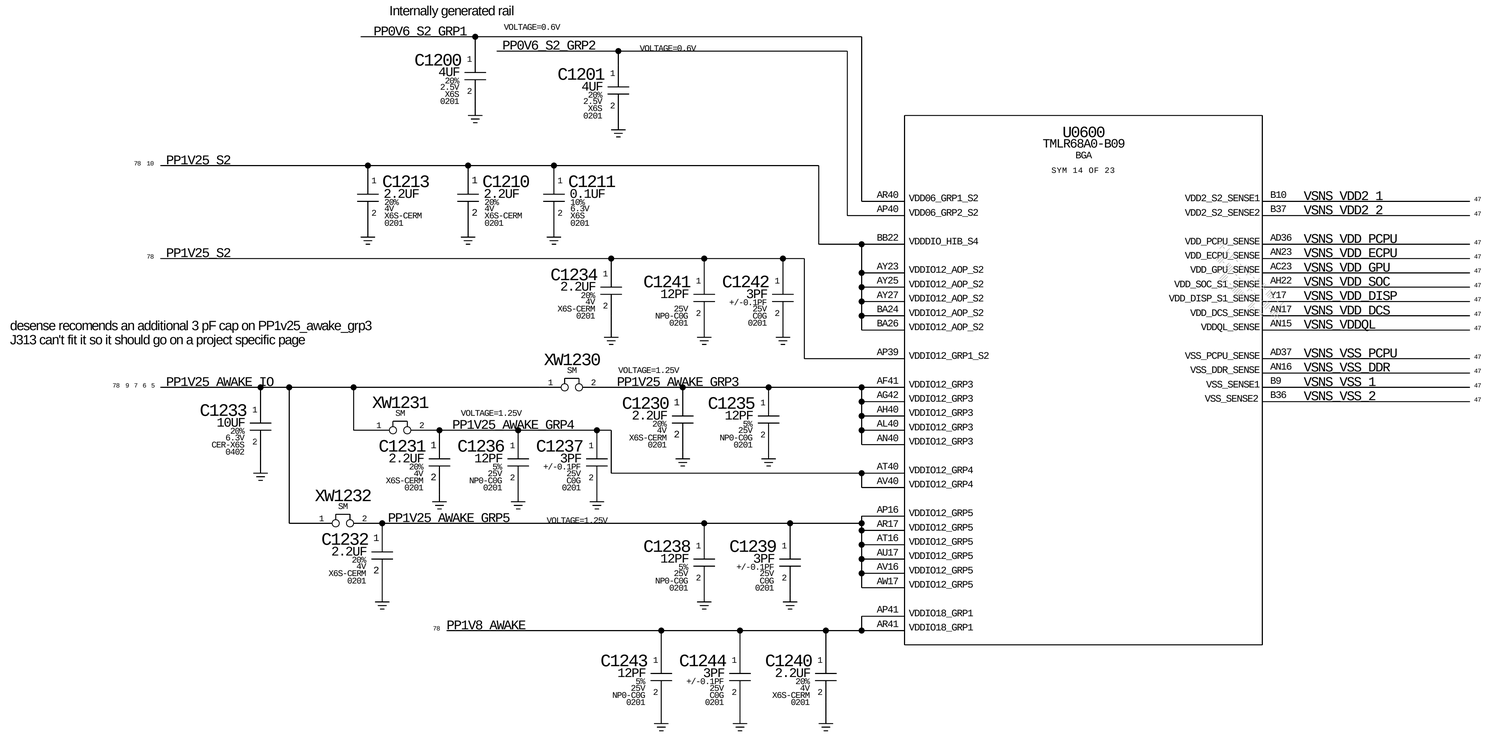
OK2INTEGRATE

SOC: POWER (IO)



BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE
SOC: POWER (IO)

Apple Inc.

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OK2INTEGRATE

SOC: POWER (CPU, GPU)

U0600
TMLR68A0-B09
BGA
SYM 11 OF 23

U0600
TMLR68A0-B09
BGA
SYM 12 OF 23

0.575V @ 4400MA

PPVDD_PCPU_AWAKE
PPVDD_GPU_AWAKE
PPVDD_ECPU_AWAKE
PPVDD_SOC_S1
PPVDD_DISP_S1

C1300 3PF +/-0.1PF 25V C0G 0201
C1301 12PF 5% 25V NP0-C0G 0201
C1340 12PF 5% 25V NP0-C0G 0201
C1341 3PF +/-0.1PF 25V C0G 0201
C1370 12PF 5% 25V NP0-C0G 0201

C1310 C1311 C1312 C1313 C1314 C1315 C1316 C1317 C1318 C1319
C1320 C1321 C1322 C1323 C1324 C1325
C1330 C1331 C1332 C1333 C1334 C1335 C1336 C1337
C1350 C1351 C1352
C1353 C1354 C1355 C1356 C1357
C1361 C1362 C1363 C1364
C1365 C1366

11UF 20% 2.5V X6T 0402

BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE: SOC: POWER (SOC, CPU, GPU)

Apple Inc.

DRAWING NUMBER: 051-05392
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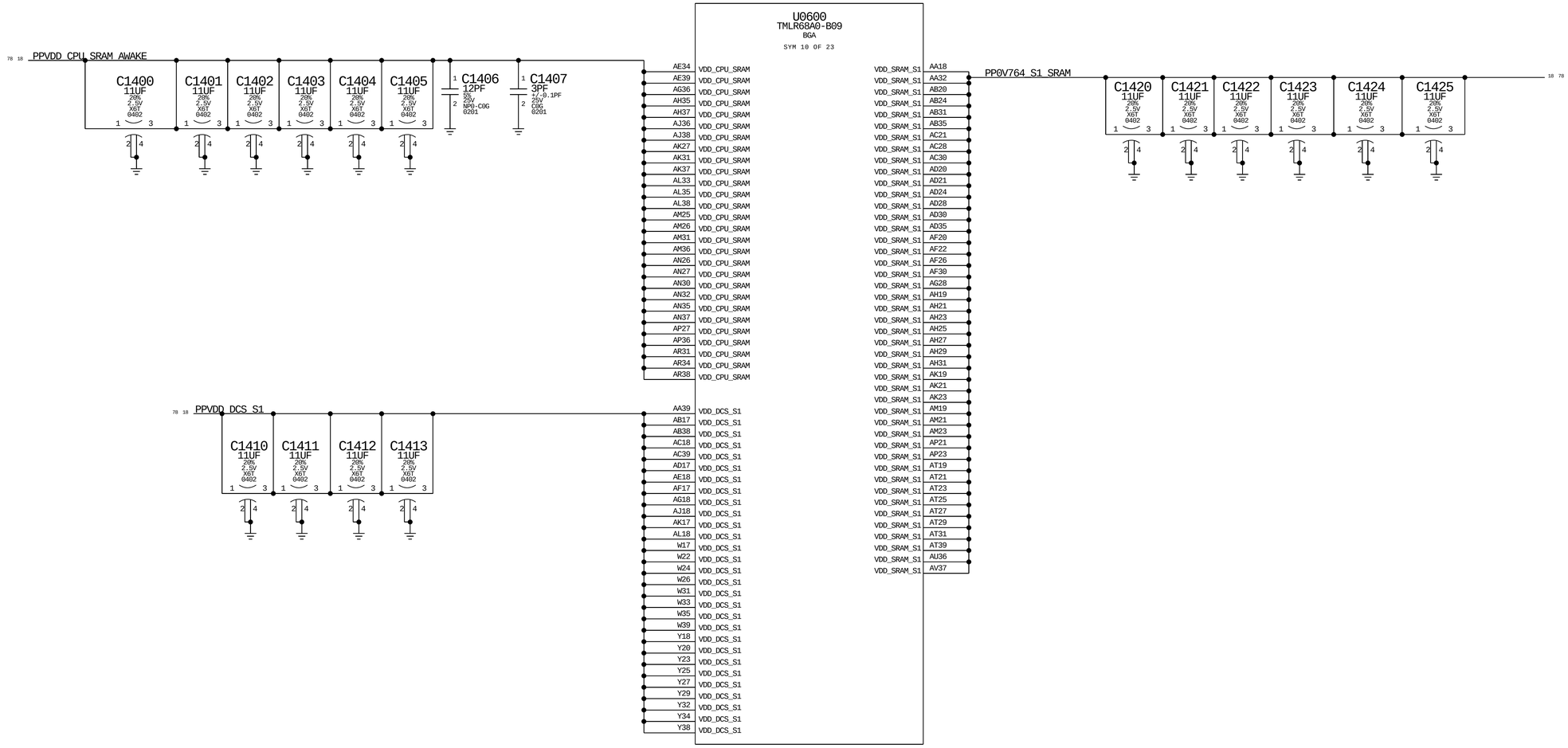
OK2INTEGRATE

SOC: POWER (SRAM, SOC)



SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE

SOC: POWER (SRAM)

Apple Inc.

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OK2INTEGRATE

U0600
TMLR68AG-B09
BGA
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PP0V805_S1_VDD_FIXED
LPDP_RX Power may be grounded,
Wait until Dev Bringup is complete before grounding it.
Until then connect it to PP1V2_AWAKE

C1505 0.1UF 10% 6.3V X6S 0201
C1506 2.2UF 20% 4V X6S-CERM 0201
C1518 12PF 5% 25V NP0-C0G 0201
C1519 3PF +/-0.1PF 25V C0G 0201
C1507 2.2UF 20% 4V X6S-CERM 0201
C1508 0.1UF 10% 6.3V X6S 0201

R1500 0 5% 1/20W ME 0201 — VOLTAGE=0.805V — PP0V805_S1_SOC_VDDFIXEDPCIE_R
C1500 2.2UF 20% 4V X6S-CERM 0201
C1501 0.1UF 10% 6.3V X6S 0201
C1513 4.3UF 20% 2.5V X6T 0402
C1514 0.1UF 10% 6.3V X6S 0201
C1515 0.1UF 10% 6.3V X6S 0201

C1502 0.1UF 10% 6.3V X6S 0201
C1503 0.1UF 10% 6.3V X6S 0201
C1504 2.2UF 20% 4V X6S-CERM 0201

FL1510 1200HM-25%-0.25A-0.50HM 0201 — VOLTAGE=0.805V — PP0V805_S1_SOC_VDDFIXEDPLL_F
C1510 2.2UF 20% 4V X6S-CERM 0201
C1511 2.2UF 20% 4V X6S-CERM 0201
C1512 0.1UF 10% 6.3V X6S 0201
C1516 0.1UF 10% 6.3V X6S 0201
C1517 0.22UF 10% 6.3V X6S-CERM 0201

R1590 10 5% 1/20W ME 201 — VOLTAGE=0.805V — PP0V805_S1_SOC_VDDFIXEDXTAL_R
C1590 4UF 20% 2.5V X6S 0201

C1520 3PF +/-0.1PF 25V C0G 0201
C1521 2.2UF 20% 4V X6S-CERM 0201

C1530 4.3UF 20% 2.5V X6T 0402
C1531 4.3UF 20% 2.5V X6T 0402

R1535 10 5% 1/20W ME 201 — VOLTAGE=0.72V — PP0V72_S2_VDD_LOWFLPLL_R
C1535 0.22UF 20% 6.3V X6S-CERM 0201

R1536 49.9 1% 1/20W ME 201 — VOLTAGE=0.72V — PP0V72_S2_VDD_LOWULPPLL_R
C1536 4UF 20% 2.5V X6S 0201

C1537 0.1UF 10% 6.3V X6S 0201

AM28	VDD_FIXED_ECPU_S1	
AW19	VDD_FIXED_LPDP_RX_S1	PP0V805_S1_VDD_FIXED
AW20	VDD_FIXED_LPDP_RX_S1	
AW21	VDD_FIXED_LPDP_RX_S1	
BA37	VDD_FIXED_LPDP_TX_S1	
BA38	VDD_FIXED_LPDP_TX_S1	
BA39	VDD_FIXED_LPDP_TX_S1	
R11	VDD_FIXED_MIPIC_S1	
R12	VDD_FIXED_MIPIC_S1	
R13	VDD_FIXED_MIPIC_S1	
R10	VDD_FIXED_MIPID_PLL_S1	
P9	VDD_FIXED_MIPID_S1	PP0V805_S1_VDD_FIXED
R9	VDD_FIXED_MIPID_S1	
AY18	VDD_FIXED_MTR_S1	
AV33	VDD_FIXED_PCIE_REFBUF_S1	
AV29	VDD_FIXED_PCIE_S1	
AV30	VDD_FIXED_PCIE_S1	
AV31	VDD_FIXED_PCIE_S1	
AV32	VDD_FIXED_PCIE_S1	
AL34	VDD_FIXED_PCPU_S1	PP0V805_S1_VDD_FIXED
AT32	VDD_FIXED_PLL_ANE_S1	
AF29	VDD_FIXED_PLL_GPU_S1	
AR20	VDD_FIXED_PLL_SOC_S1	
AH13	VDD_FIXED_PLL_DDR0_S1	
AG13	VDD_FIXED_PLL_DDR1_S1	
AC13	VDD_FIXED_PLL_DDR2_S1	
T24	VDD_FIXED_PLL_DDR3_S1	
R28	VDD_FIXED_PLL_DDR4_S1	
R29	VDD_FIXED_PLL_DDR5_S1	
T34	VDD_FIXED_PLL_DDR6_S1	
AC42	VDD_FIXED_PLL_DDR7_S1	
BA32	VDD_FIXED_XTAL_S1	
AD40	VDD_FIXED_S1	
AG40	VDD_FIXED_S1	
AJ39	VDD_FIXED_S1	
AP17	VDD_FIXED_S1	
AU32	VDD_FIXED_S1	
AV39	VDD_FIXED_S1	
AY16	VDD_FIXED_S1	
V17	VDD_FIXED_S1	
AV23	VDD_LOW_S2	
AV25	VDD_LOW_S2	
AV27	VDD_LOW_S2	
AW26	VDD_LOW_S2	
AY26	VDD_LOW_S2	
BA23	VDD_LOW_S2	PP0V72_S2_VDD_LOW
AW24	VDD_LOW_FLPPLL_S2	
AW22	VDD_LOW_ULPPLL_S2	
AW28	VDD_LOW_USB_DEBUG_S2	
BA22	VDD_HIB_S4	

AV34	VDD_CIO	PP0V855_S2SW_CIO
AV36	VDD_CIO	
AW35	VDD_CIO	
AU42	VDD12_CIO_S2	PP1V2_S2_CIO
AU43	VDD12_CIO_S2	
AV42	VDD12_CIO_S2	
AV43	VDD12_CIO_S2	
AV34	VDD12_CIO_S2	
AV36	VDD12_CIO_S2	
BA35	VDD12_CIO_S2	
AU34	VDD_CIO_USB	
AU35	VDD12_CIO_USB_S2	
AT42	VDD12_AMUX_S2	PP0V855_S2SW_CIO
AV11	VDD12_LPDP_RX	PP1V2_S2_CIO
AV20	VDD12_LPDP_RX	PP1V25_S2
AW11	VDD12_LPDP_RX	PP1V25_AWAKE_IO
AW13	VDD12_LPDP_RX	
AY13	VDD12_LPDP_RX	PP1V2_AWAKE_PLL
AY19	VDD12_LPDP_RX	
AY20	VDD12_LPDP_RX	
AY21	VDD12_LPDP_RX	
AW37	VDD12_LPDP_TX	
AW38	VDD12_LPDP_TX	
AW39	VDD12_LPDP_TX	
P11	VDD12_MIPIC	PP1V25_AWAKE_IO
P12	VDD12_MIPIC	
P13	VDD12_MIPIC	
P8	VDD12_MIPID	
R8	VDD12_MIPID	
AW18	VDD12_MTR	PP1V25_AWAKE_IO
AY29	VDD12_PCIE	PP1V2_AWAKE_PLL
AY30	VDD12_PCIE	
AY31	VDD12_PCIE	
AY32	VDD12_PCIE	
AY43	VDD12_PCIE	
BA42	VDD12_PCIE	
BA43	VDD12_PCIE	
AW33	VDD12_PCIE_REFBUF	VOLTAGE=1.2V — PP1V2_AWAKE_PLL_PCIE_R
AP31	VDD12_PLL_ANE	
AK34	VDD12_PLL_CPU	
AG29	VDD12_PLL_GPU	
AP19	VDD12_PLL_SOC	PP1V2_AWAKE_PLL
AK32	VDD12_TSADC_CPU	
U29	VDD12_TSADC_SOC0	PP1V25_AWAKE_IO
Y33	VDD12_TSADC_SOC1	
AH32	VDD12_TSADC_SOC2	
AV15	VDD12_TSADC_SOC3	VOLTAGE=1.25V — PP1V25_S2_ULPPLL_R
AE40	VDD12_TSADC_SOC4	
AW23	VDD12_ULPPLL_S2	PP1V25_S2
AY28	VDD12_USB_DEBUG_S2	
BA33	VDD12_XTAL	
AU40	VDD12_EFUSE1	VOLTAGE=1.25V — PP1V25_AWAKE_XTAL_F
AT20	VDD12_EFUSE2	
AB43	VDD12_EFUSE3	
AU19	VDD12_FMON	VOLTAGE=1.25V — PP1V25_AWAKE_FMON_R

C1540 0.1UF 10% 6.3V X6S 0201
C1541 0.1UF 10% 6.3V X6S 0201
C1542 4.3UF 20% 2.5V X6T 0402
C1543 4.3UF 20% 2.5V X6T 0402
C1544 0.1UF 10% 6.3V X6S 0201
C1545 0.1UF 10% 6.3V X6S 0201
C1546 4.3UF 20% 2.5V X6T 0402
C1547 4.3UF 20% 2.5V X6T 0402

C1563 3PF +/-0.1PF 25V C0G 0201
C1564 12PF 5% 25V NP0-C0G 0201
C1550 2.2UF 20% 4V X6S-CERM 0201
C1551 0.1UF 10% 6.3V X6S 0201

LPDP_RX Power may be grounded,
Wait until Dev Bringup is complete before grounding it.
Until then connect it to PP1V2_AWAKE

C1560 2.2UF 20% 4V X6S-CERM 0201
C1561 0.1UF 10% 6.3V X6S 0201
C1562 2.2UF 20% 4V X6S-CERM 0201

C1553 0.1UF 10% 6.3V X6S 0201
C1554 0.1UF 10% 6.3V X6S 0201
C1555 4.3UF 20% 2.5V X6T 0402
C1556 4.3UF 20% 2.5V X6T 0402

R1574 0 5% 1/20W ME 0201
C1573 0.1UF 10% 6.3V X6S 0201
C1574 2.2UF 20% 4V X6S-CERM 0201

C1570 0.1UF 10% 6.3V X6S 0201
C1571 0.1UF 10% 6.3V X6S 0201
C1572 2.2UF 20% 4V X6S-CERM 0201

R1584 49.9 1% 1/20W ME 201
C1584 4.7UF 20% 6.3V CER 0402
C1582 0.1UF 10% 6.3V X6S 0201

FL1580 240-OHM-0.2A-0.9-OHM 0201
C1580 0.1UF 10% 6.3V X6S 0201
C1581 2.2UF 20% 4V X6S-CERM 0201

R1583 49.9 1% 1/20W ME 201
C1583 2.2UF 20% 4V X6S-CERM 0201

SYNC_MASTER=rwf_soc_h13g — SYNC_DATE=05/04/2020

PAGE TITLE
$SOC: POWER (Fixed, PLL's, Filtered)

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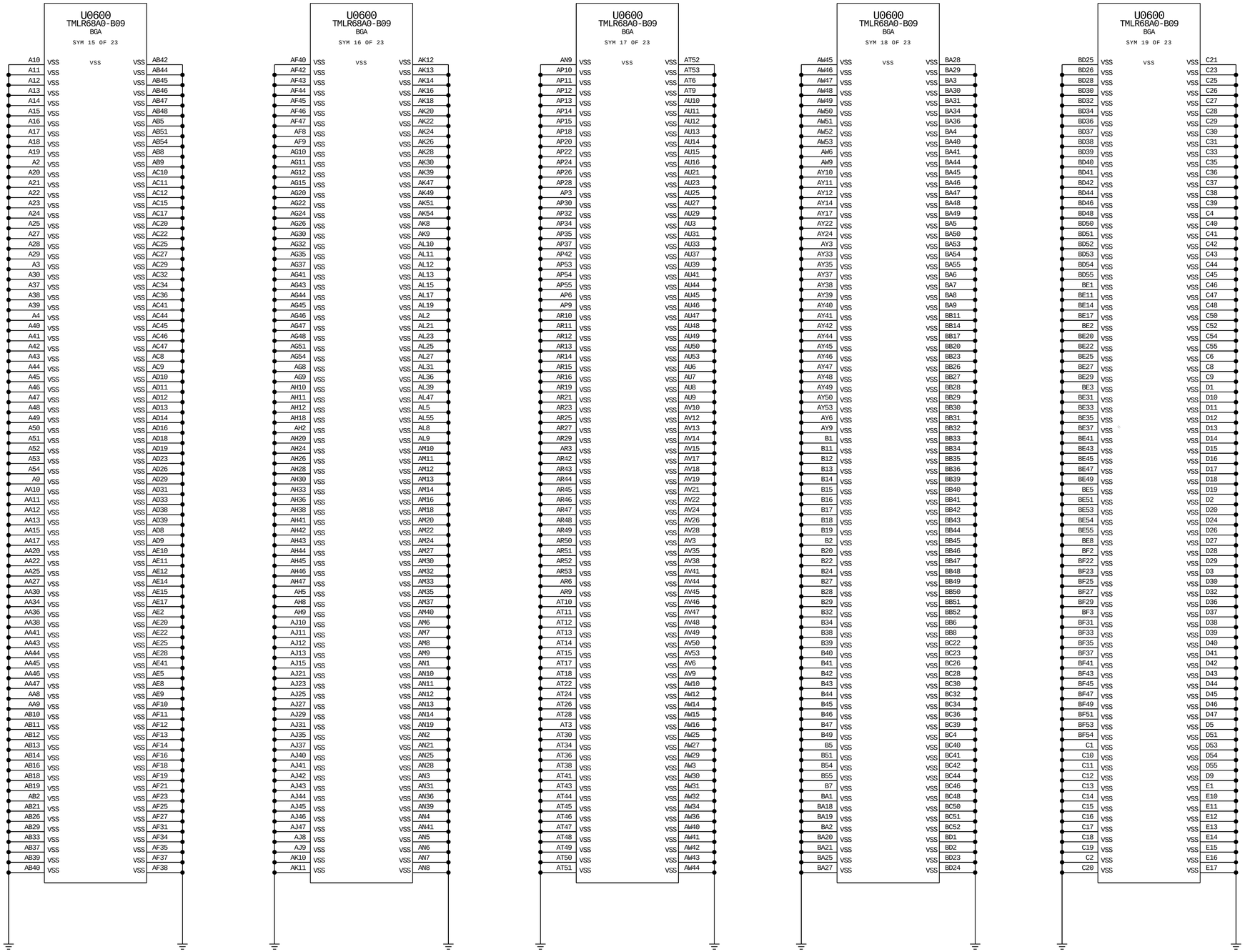
OK2INTEGRATE

SOC: GND (1)



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SYNC_MASTER=ref_soc_513g SYNC_DATE=05/04/2020

PAGE TITLE

SOC: GND

Apple Inc.

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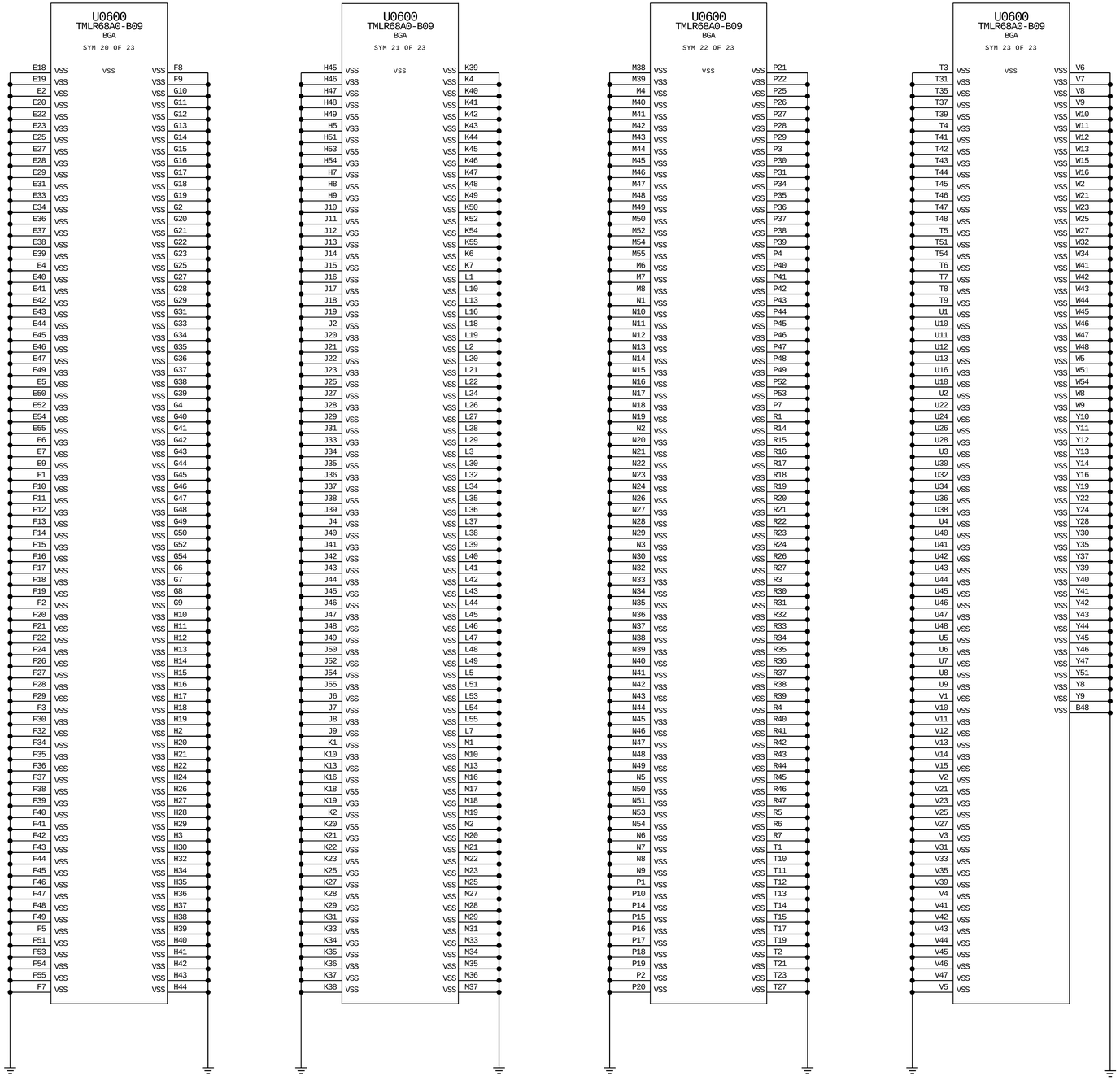
OK2INTEGRATE

SOC: GND (2)



SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE

SOC: GND-2

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78 11 PP1V8_S2SW_VDD1

C1800 12PF 5% 25V NP0-C0G 0201
C1801 3.0PF +/-0.1PF 25V NP0-C0G 0201
C1802 12PF 5% 25V NP0-C0G 0201
C1803 3.0PF +/-0.1PF 25V NP0-C0G 0201
C1804 12PF 5% 25V NP0-C0G 0201
C1805 3.0PF +/-0.1PF 25V NP0-C0G 0201

78 11 PP1V06_S2SW_DRAM

C1810 12PF 5% 25V NP0-C0G 0201
C1811 3.0PF +/-0.1PF 25V NP0-C0G 0201
C1812 12PF 5% 25V NP0-C0G 0201
C1813 3.0PF +/-0.1PF 25V NP0-C0G 0201
C1814 12PF 5% 25V NP0-C0G 0201
C1815 3.0PF +/-0.1PF 25V NP0-C0G 0201

78 11 PP0V6_S1_VDDQL

C1820 12PF 5% 25V NP0-C0G 0201
C1821 3.0PF +/-0.1PF 25V NP0-C0G 0201
C1822 12PF 5% 25V NP0-C0G 0201
C1823 3.0PF +/-0.1PF 25V NP0-C0G 0201
C1824 12PF 5% 25V NP0-C0G 0201
C1825 3.0PF +/-0.1PF 25V NP0-C0G 0201

78 13 PPVDD_PCPU_AWAKE

C1830 12PF 5% 25V NP0-C0G 0201
C1831 3.0PF +/-0.1PF 25V NP0-C0G 0201
C1832 12PF 5% 25V NP0-C0G 0201
C1833 3.0PF +/-0.1PF 25V NP0-C0G 0201
C1834 12PF 5% 25V NP0-C0G 0201
C1835 3.0PF +/-0.1PF 25V NP0-C0G 0201

78 13 PPVDD_GPU_AWAKE

C1840 12PF 5% 25V NP0-C0G 0201
C1841 3.0PF +/-0.1PF 25V NP0-C0G 0201
C1842 12PF 5% 25V NP0-C0G 0201
C1843 3.0PF +/-0.1PF 25V NP0-C0G 0201
C1844 12PF 5% 25V NP0-C0G 0201
C1845 3.0PF +/-0.1PF 25V NP0-C0G 0201

78 14 PPVDD_CPU_SRAM_AWAKE

C1850 12PF 5% 25V NP0-C0G 0201
C1851 3.0PF +/-0.1PF 25V NP0-C0G 0201
C1852 12PF 5% 25V NP0-C0G 0201
C1853 3.0PF +/-0.1PF 25V NP0-C0G 0201

78 14 PPVDD_DCS_S1

C1854 12PF 5% 25V NP0-C0G 0201
C1855 3.0PF +/-0.1PF 25V NP0-C0G 0201
C1856 12PF 5% 25V NP0-C0G 0201
C1857 3.0PF +/-0.1PF 25V NP0-C0G 0201

78 14 PP0V764_S1_SRAM

C1860 12PF 5% 25V NP0-C0G 0201
C1861 3.0PF +/-0.1PF 25V NP0-C0G 0201
C1862 12PF 5% 25V NP0-C0G 0201
C1863 3.0PF +/-0.1PF 25V NP0-C0G 0201

78 15 PP0V805_S1_VDD_FIXED

C1864 12PF 5% 25V NP0-C0G 0201
C1865 3.0PF +/-0.1PF 25V NP0-C0G 0201

78 19 PP0V805_S1_VDD_FIXED

C1866 12PF 5% 25V NP0-C0G 0201
C1867 3.0PF +/-0.1PF 25V NP0-C0G 0201

78 15 PP0V72_S2_VDD_LOW

C1870 12PF 5% 25V NP0-C0G 0201
C1871 3.0PF +/-0.1PF 25V NP0-C0G 0201

78 13 PPVDD_ECPU_AWAKE

C1872 12PF 5% 25V NP0-C0G 0201
C1873 3.0PF +/-0.1PF 25V NP0-C0G 0201

78 13 PPVDD_DISP_S1

C1874 3.0PF +/-0.1PF 25V NP0-C0G 0201

BOM_COST_GROUP=DESENSE

SYNC_MASTER=ref_soc_h13g SYNC_DATE=10/08/2019

PAGE TITLE: SOC: DESENSE CAPS

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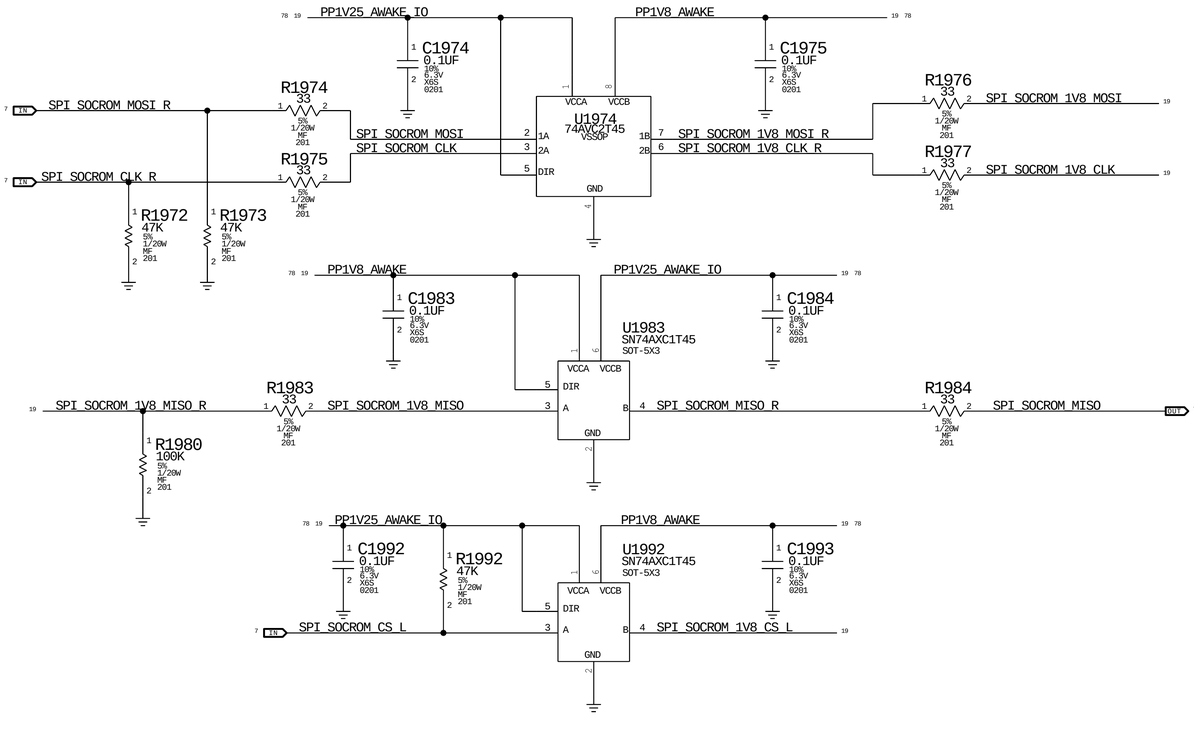
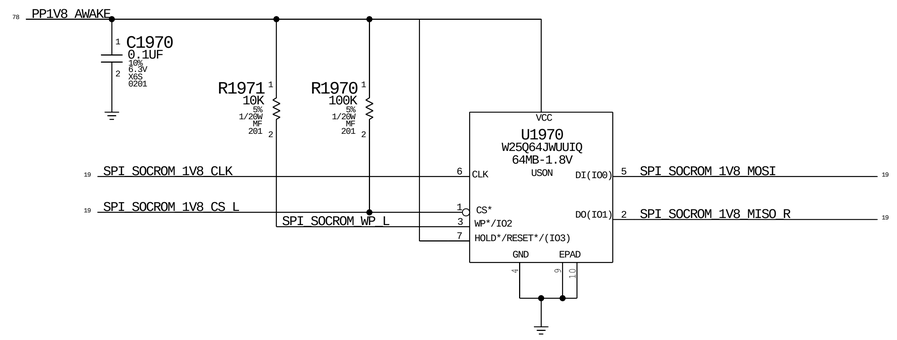
OK2INTEGRATE

SPI NOR (1.8V 64 M-BIT)





BOM_COST_GROUP=SOC

SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE: SPI NOR

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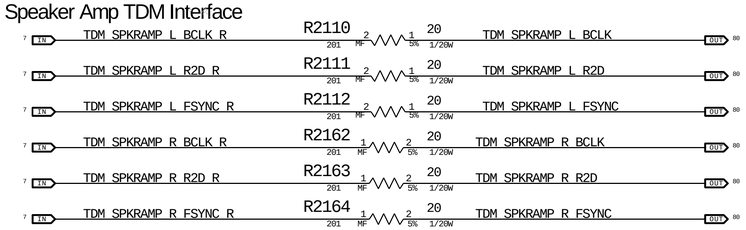
A Series Terminations

TCON SPI Interface

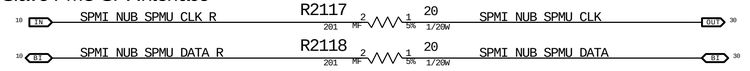
Speaker Amp TDM Interface



Trackpad SPI Interface

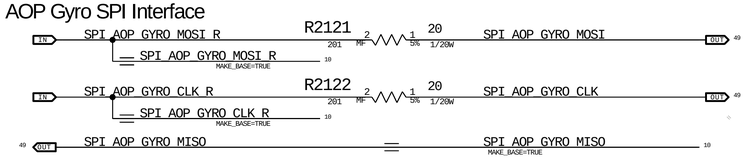
Master PMU SPI Interface

Slave PMU SPI Interface



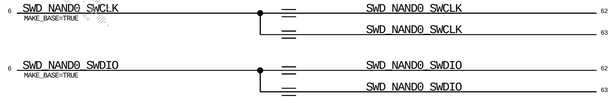
SPMI Interface

AOP Gyro SPI Interface

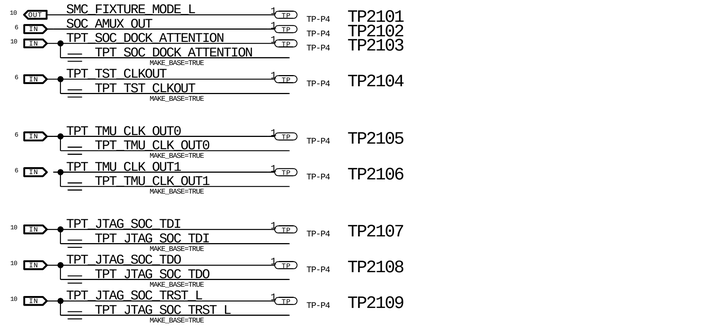


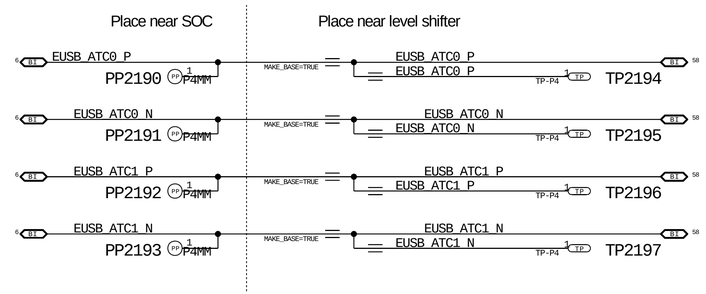
B BOOT Config Aliases

C SSD S5E Data/Clock Aliases

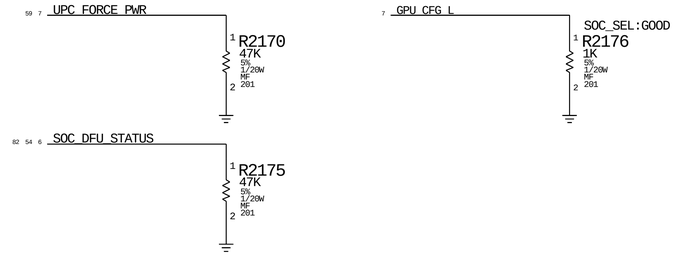


D Test Points





E Pull Down Resistors



SYNC_MASTER=ref_soc_h13g SYNC_DATE=05/04/2020

PAGE TITLE

SOC: Project Support

Apple Inc.

DRAWING NUMBER 051-05392 SIZE D

REVISION 4.0.0

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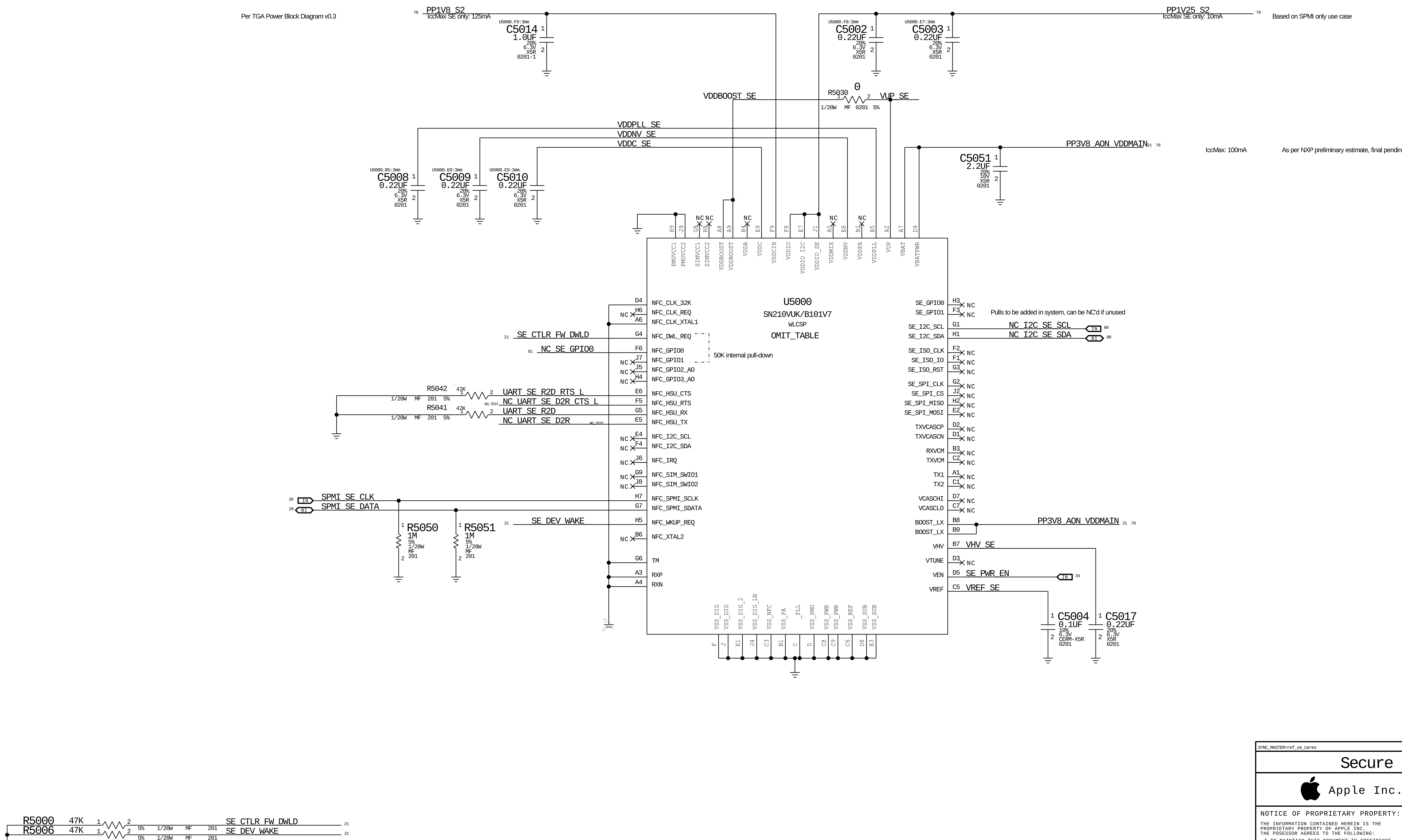
Timing Requirements:
- VBAT supply ramp time: 20ms

Ceres - Secure Element

*** OK2INTEGRATE ***



Per TGA Power Block Diagram v0.3
PP1V8_S2
IccMax SE only: 125mA
PP1V25_S2
IccMax SE only: 10mA
Based on SPMI only use case
C5014 1.0UF 20% 6.3V X5R 0201-1
C5002 0.22UF 20% 6.3V X5R 0201
C5003 0.22UF 20% 6.3V X5R 0201
VDDBOOST_SE
R5030 0 1/20W MF 0201 5%
VUP_SE
VDDPLL_SE
VDDNV_SE
VDDC_SE
PP3V8_AON_VDDMAIN
IccMax: 100mA
As per NXP preliminary estimate, final pending
C5051 2.2UF 20% 10V X5R 0201
C5008 0.22UF 20% 6.3V X5R 0201
C5009 0.22UF 20% 6.3V X5R 0201
C5010 0.22UF 20% 6.3V X5R 0201
U5000
SN210VUK/B101V7
WLCSP
OMIT_TABLE
NFC_CLK_32K
NFC_CLK_REQ
NFC_CLK_XTAL1
NFC_DWL_REQ
NFC_GPIO0
NFC_GPIO1
NFC_GPIO2_AO
NFC_GPIO3_AO
NFC_HSU_CTS
NFC_HSU_RTS
NFC_HSU_RX
NFC_HSU_TX
NFC_I2C_SCL
NFC_I2C_SDA
NFC_IRQ
NFC_SIM_SWIO1
NFC_SIM_SWIO2
NFC_SPMI_SCLK
NFC_SPMI_SDATA
NFC_WKUP_REQ
NFC_XTAL2
TM
RXP
RXN
SE_CTLR_FW_DWLD
NC_SE_GPIO0
50K internal pull-down
R5042 47K 1/20W MF 201 5%
UART_SE_R2D_RTS_L
NC_UART_SE_D2R_CTS_L
R5041 47K 1/20W MF 201 5%
UART_SE_R2D
NC_UART_SE_D2R
SPMI_SE_CLK
SPMI_SE_DATA
SE_DEV_WAKE
R5050 1M 5% 1/20W MF 201
R5051 1M 5% 1/20W MF 201
SE_GPIO0
SE_GPIO1
Pulls to be added in system, can be NC'd if unused
SE_I2C_SCL
SE_I2C_SDA
NC_I2C_SE_SCL
NC_I2C_SE_SDA
SE_ISO_CLK
SE_ISO_IO
SE_ISO_RST
SE_SPI_CLK
SE_SPI_CS
SE_SPI_MISO
SE_SPI_MOSI
TXVCASCP
TXVCASCN
RXVCM
TXVCM
TX1
TX2
VCASCHI
VCASCLO
BOOST_LX
VHV
VTUNE
VEN
VREF
VHV_SE
SE_PWR_EN
VREF_SE
C5004 0.1UF 10% 6.3V CERM-X5R 0201
C5017 0.22UF 20% 6.3V X5R 0201
PMUVCC1
PMUVCC2
SIMVCC1
SIMVCC2
VDDBOOST
VDDA
VDDC
VDDCIN
VDDIO
VDDIO_I2C
VDDIO_SE
VDDMIX
VDDNV
VDDPA
VDDPLL
VUP
VBAT
VBATPWR
VSS_DIG
VSS_DIG_2
VSS_DIG_LN
VSS_NFC
VSS_PA
VSS_PLL
VSS_PMU
VSS_PWR
VSS_REF
VSS_SUB
R5000 47K
R5006 47K 5% 1/20W MF 201
SE_CTLR_FW_DWLD
SE_DEV_WAKE

<rdar://problem/52067756> [SN200V] Wired Mode SE Only Reference Design Material
<rdar://problem/45108950> Mac - Venus Reference guide and De-coupling requirements

BOM_COST_GROUP=SECURE ELEMENT

SYNC_MASTER=ref_se_ceres SYNC_DATE=03/29/2020

Secure Element	
Apple Inc.	DRAWING NUMBER 051-05392 SIZE D
	REVISION 4.0.0
NOTICE OF PROPRIETARY PROPERTY:	BRANCH evt-1
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	PAGE 50 OF 801
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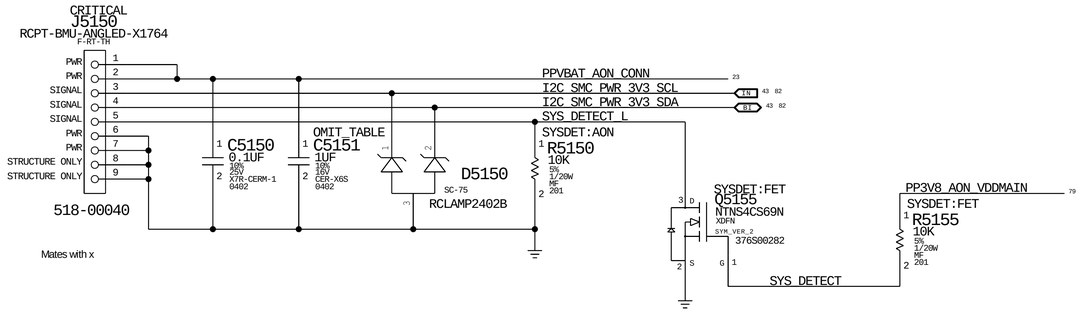

BMU output is enabled after power is
supplied by other means, such as USBC connector.
MLB is thus unpowered during system assembly.

SYNC_MASTER=ref_se_ceres SYNC_DATE=03/29/2020

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BMU Connector, Btn Logic

Apple Inc.

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*** OK2INTEGRATE ***

PPDCIN_AON_CHGR_R
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1800
VOLTAGE=20V

CRITICAL C5201 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM CAPMAT=POLY-TANT
CRITICAL C5202 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM CAPMAT=POLY-TANT
CRITICAL C5203 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM CAPMAT=POLY-TANT
CRITICAL C520A 2.2UF 20% 35V X5R-CERM 0402
CRITICAL C520B 2.2UF 20% 35V X5R-CERM 0402
CRITICAL C520C 2.2UF 20% 35V X5R-CERM 0402
CRITICAL C520D 2.2UF 20% 35V X5R-CERM 0402
CRITICAL C5204 6.8UF 20% 35V-0.090HM POLY-TANT CASE-B1-2-SM CAPMAT=POLY-TANT

FROM USB-C SOURCE

79 23 PPDCIN_AONSW

CRITICAL R5220 0.01 0.5% 0.5W MF 0306
NO_XNET_CONNECTION=1
(AMON) 1-CELL: 0.02 OHM 3-CELL: 0.01 OHM
107S00053

PP5211 P2MM SM 1 CHGR_GATE_Q1 23 PLACE_SIDE=BOTTOM
PP5212 P2MM SM 1 CHGR_GATE_Q2 23 PLACE_SIDE=BOTTOM
PP5213 P2MM SM 1 CHGR_GATE_Q3 23 PLACE_SIDE=BOTTOM
PP5214 P2MM SM 1 CHGR_GATE_Q4 23 PLACE_SIDE=BOTTOM
PP5215 P2MM SM 1 CHGR_PHASE1 23 PLACE_SIDE=BOTTOM
PP5216 P2MM SM 1 CHGR_PHASE2 23 PLACE_SIDE=BOTTOM
PP5207 P2MM SM 1 CHGR_EN_MVR 23 PACK_OPTION=CHGR_TP
PP5208 P2MM SM 1 CHGR_INT_1V8_L 23 24 PACK_OPTION=CHGR_TP

CHGR_CSI_P — PLACE_NEAR=U5200.D5:2MM
R5221 1.00 1% 1/20W MF-LF 0201
CHGR_CSI_N — PLACE_NEAR=U5200.C5:2MM
R5222 1.00 1% 1/20W MF-LF 0201
CHGR_CSI_FILT_P
CRITICAL C5221 0.047UF 10% 50V CER-X7R 0402
CHGR_CSI_FILT_N
CRITICAL C5222 0.047UF 10% 50V CER-X7R 0402

CRITICAL C5220 0.47UF 20% 6.3V CERM-X5R-1 201 NO_XNET_CONNECTION=1

23 PPVBAT_AON_CHGR_REG
C5278 2.2UF 20% 35V X5R-CERM 0402

79 23 PPDCIN_AONSW
R5215 750K 1% 1/20W MF 201
CHGR_AUX_DET
NOSTUFF C5216 0.01UF 10% 25V X5R-CERM 0201
R5216 255K 1% 1/20W MF 201

78 24 PP1V8_S2
C5280 1.0UF 20% 6.3V X5R 0201-1

CRITICAL L5230 2.7UH-20%-12.5A-0.01960HM
IHLP4848BD-PIMA102D-COMBO 152S00198
23 CHGR_PHASE1 DIDT=TRUE SWITCH_NODE=TRUE
CHGR_PHASE2 23 SWITCH_NODE=TRUE

CRITICAL Q5230 SIZ342DT PWRPAIR-3X3-COMBO (G1)
CRITICAL Q5240 SIZ342DT PWRPAIR-3X3-COMBO (G2)
CRITICAL ALLOW_APPLE_PREFIX=Q

23 CHGR_GATE_Q1 DIDT=TRUE SWITCH_NODE=TRUE
23 CHGR_GATE_Q2 DIDT=TRUE GATE_NODE=TRUE
CHGR_GATE_Q3 23 DIDT=TRUE GATE_NODE=TRUE
CHGR_GATE_Q4 23 DIDT=TRUE SWITCH_NODE=TRUE

CHGR_LX1 DIDT=TRUE SWITCH_NODE=TRUE
CRITICAL C5230 0.1UF 10% 25V X7R-CERM-1 0402
CHGR_BOOT1_RC DIDT=TRUE SWITCH_NODE=TRUE
R5230 0 5% 1/10W MF-LF 402
CHGR_BOOT1 DIDT=TRUE SWITCH_NODE=TRUE

XW5230 SM
XW5240 SM

CHGR_LX2 DIDT=TRUE SWITCH_NODE=TRUE
CRITICAL C5240 0.1UF 10% 25V X7R-CERM-1 0402
CHGR_BOOT2_RC DIDT=TRUE SWITCH_NODE=TRUE
R5240 0 5% 1/10W MF-LF 402
CHGR_BOOT2 DIDT=TRUE SWITCH_NODE=TRUE

XW5260 SM PLACE_NEAR=Q5240.3:2MM

R5275 4.7 5% 1/20W MF 201
VOLTAGE=5V PPCHGR_VDDA
CRITICAL C5275 2.2UF 20% 25V X5R-CERM 0402-1
VOLTAGE=5V PPCHGR_VDDP
CRITICAL C5277 10UF 20% 10V X5R 0603-1

U5200 ISL9240HI WCSP
SCH SYMBOL 353S01525
CRITICAL

B5	P_IN	GATE_Q1	H1
C5	CSIN	BOOT1	F1
D5	CSIP	LX1	G1
A5	PBUS_PWR	GATE_Q2	E1
D3	AUX_DET	GATE_Q3	D1
		LX2	B1
		BOOT2	C1
		GATE_Q4	A1
		PBUS	A3 — CHGR_PBUS_SNS (MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000)
		CSOP	A4
		CSON	B4
		BGATE	B3 — CHGR_BGATE
		VBAT	C3 — CHGR_VBAT
		EN_VR1	F2 — NC_CHGR_EN_VR1 (01)
		SMC_RST*	H4 — NC_CHGR_SMC_RST_L (01)
		IRQ*	H3 — CHGR_INT_1V8_L (OUT 23 24)
		CBC_ON	H2 — NC_CHGR_CBC_ON (01)
F5	VDDIO1P8	(5V) EN_MVR	F4 — CHGR_EN_MVR (OUT 23 24)
G5	SDA	(OD) AUX_OK	F3 — CHGR_AUX_OK (OUT 24)
H5	SCL	AMON	D4 — CHGR_AMON (OUT 44)
G2	SMC_RST_IN	BMON	C4 — CHGR_BMON (OUT 44)
G3	HPWR_EN*		
E5	COMP		
G4	CELL		
B2	NC0		
C2	NC1		
E4	NC2		

43 B1 I2C_SMC_PWR_1V8_SDA
43 IN I2C_SMC_PWR_1V8_SCL
35 IN CHGR_RST_IN
CHGR_COMP
H3:CELL L2:CELL

CRITICAL C5270 0.12UF 10% 10V X5R 0402
NOSTUFF CRITICAL C5271 0.12UF 10% 10V X5R 0402

CRITICAL C5254 33UF 20% 16V TANT CASED12-SM CAPMAT=POLY-TANT
CRITICAL C5255 33UF 20% 16V TANT CASED12-SM CAPMAT=POLY-TANT
CRITICAL C5256 2.2UF 20% 25V X5R 0402-1
CRITICAL C5257 2.2UF 20% 25V X5R 0402-1
C5258 1000PF 10% 25V X7R 0201
PACK_OPTION=CHGR_40W
PACK_OPTION=CHGR_40W

CRITICAL F5200 12A-32V-0.00450HM 1206

23 PPVBAT_AON_CHGR_REG
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=13.05V
TO SYSTEM
PPBUS_AON 79

PPVBAT_AON_CHGR_R
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
VOLTAGE=13.05V
CRITICAL C5265 2.2UF 20% 25V X5R 0402-1
CRITICAL C5266 2.2UF 20% 25V X5R 0402-1
CRITICAL C5267 0.1UF 10% 16V X5R 0201
CRITICAL C5268 0.01UF 10% 16V X5R-CERM 0201

NO_XNET_CONNECTION=1
CRITICAL R5260 0.005 1% 1W MF 0612-8
(PMON) 1-CELL: 0.010 OHM 3-CELL: 0.005 OHM
107S00087

CRITICAL Q5265 SI7655DN-COMBO PWRPK-1212-8 SYM-VER-2
C5264 1000PF 10% 25V X7R 0201
C5263 4700PF 10% 25V CER-XSR 0201
C5269 0.1UF 10% 25V X5R 0201
TO/FROM BATTERY
PPVBAT_AON_CONN 22
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
VOLTAGE=13.05V

CHGR_CSO_P — PLACE_NEAR=U5200.A4:2MM
R5261 1.00 1% 1/20W MF-LF 0201
CHGR_CSO_N — PLACE_NEAR=U5200.B4:2MM
R5262 1.00 1% 1/20W MF-LF 0201
CHGR_CSO_FILT_P
CRITICAL C5261 0.047UF 10% 50V CER-X7R 0402
CHGR_CSO_FILT_N
CRITICAL C5262 0.047UF 10% 50V CER-X7R 0402

CRITICAL C5260 0.47UF 20% 6.3V CERM-X5R-1 201 NO_XNET_CONNECTION=1

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

CRITICAL Q5270 <rdar://37259372&39763505>
NTNS4CS69N XDFN SYM_VER_1
SAVE_BAT_S
SAVE_BAT_G
PPDCIN_AONSW 23 79
R5271 200K 1% 1/20W MF 201
R5263 1K 5% 1/20W MF 201
R5270 24K 5% 1/20W MF 201
CRITICAL D5270 DFN0201 ALLOW_APPLE_PREFIX=D GDZ5V6LP3-55

SYNC_MASTER=ref_charger_suona
SYNC_DATE=03/29/2020

PAGE TITLE
PBUS SUPPLY & BATTERY CHARGER

Apple Inc.

DRAWING NUMBER 051-05392 SIZE D
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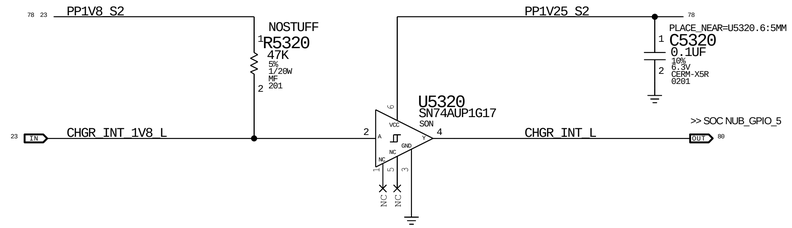
*** OK2INTEGRATE ***

CHGR I2C Level Translation

SMBUS_CHGR_1V8_[SCL/SDA]: Level translation circuit to be placed in project specific I2C page.

CHGR_INT_L Level Translation

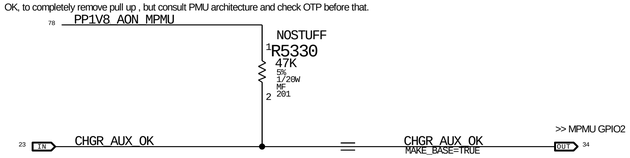
Stuff R5320 in case, glitch during power sequencing is a concern.



CHGR_AUX_OK Pull Up

Pull up to MPMU LDO9, or rely on MPMU internal pull up.

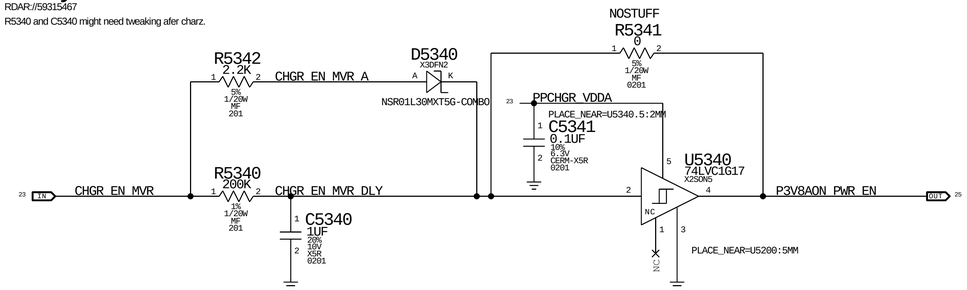
OK, to completely remove pull up , but consult PMU architecture and check OTP before that.



Delay for 3.8V VR Enable

RDAR://59315467

R5340 and C5340 might need tweaking afer charz.



BOM_COST_GROUP=BATTERY

SYNC_MASTER=ref_charger_suvna SYNC_DATE=05/02/2020

PAGE TITLE

BATTERY CHARGER SUPPORT

Apple Inc.

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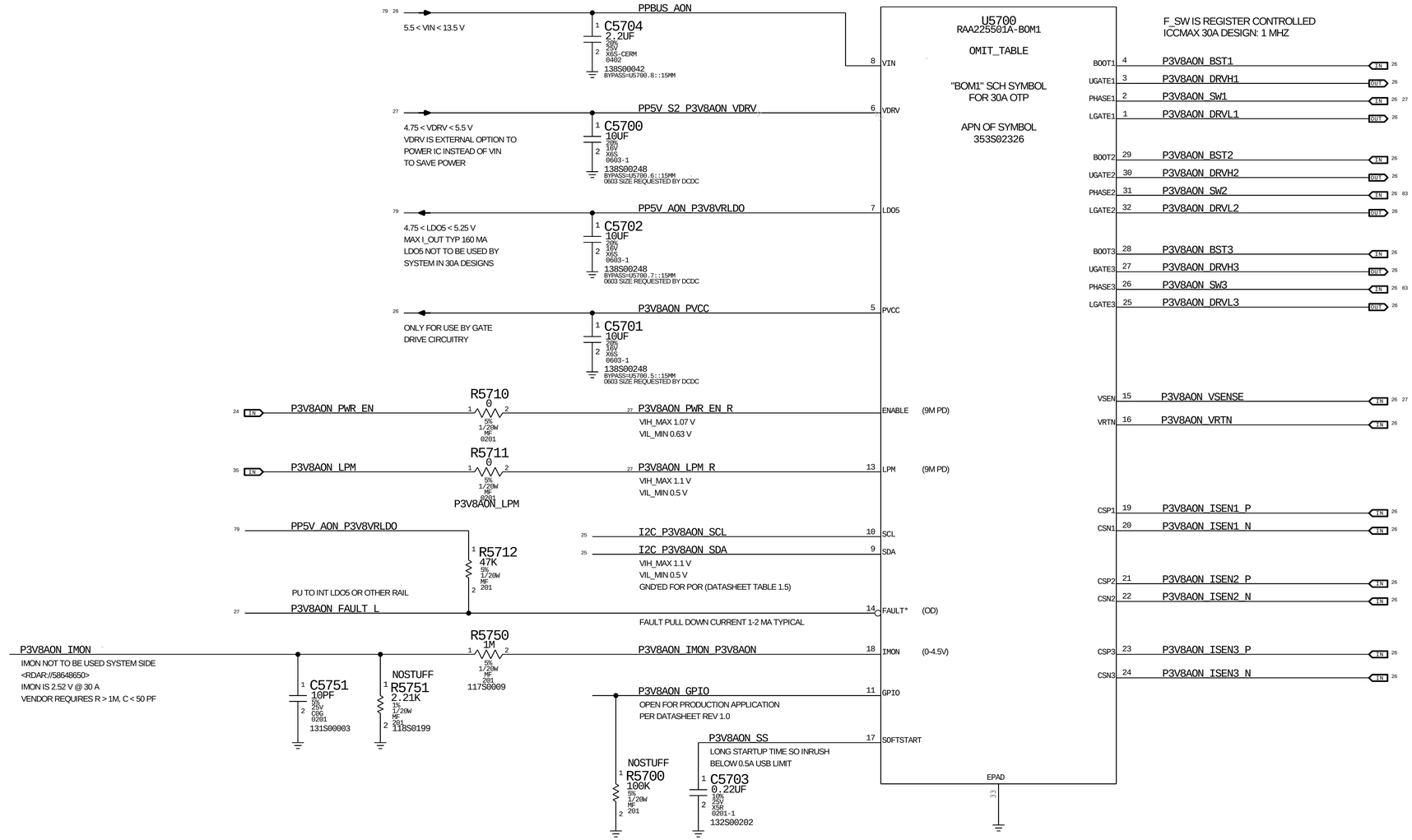
*** OK2RELEASE ***

3V8 AON CONTROLLER



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02326	1	IC,RAA225501,3-PH VOLT REG,TQFN32	U5700	CRITICAL	P3V8A0N_IC:A0
353S02472	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B0,QFN32	U5700	CRITICAL	P3V8A0N_IC:A1_R0B0

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=ref_vr_iceman
SYNC_DATE=05/02/2020

PAGE TITLE
POWER: 3V8 AON (1/2)

Apple Inc.

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SIZE D
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8 | 7 | 5 | 4

8

*** OK2RELEASE ***

PPBUS_AON

P3V8AON_DRVH1 — R5804 2.2 5% 1/20W MF 0201 117S0056 <RDAR://59524111> — P3V8AON_DRVH1_R

P3V8AON_BST1 — R5803 0 5% 1/20W MF 0201 117S0201 — P3V8AON_BST1_RC — C5811 0.1UF 10% 25V X7R-CERM-1 0402 132S0438 — P3V8AON_SW1

NOSTUFF D5800 SBR1A30T5 SOD523 3715S0245 3V8_EXT_DIODE — P3V8AON_PVCC

P3V8AON_DRVL1 — R5805 1 5% 1/16W MF-LF 402 116S0006 — P3V8AON_DRVL1_R

CRITICAL Q5800 CSD58889Q3D Q3D 376S00012 (TG, TGR, BG, VSW, VIN, GND)

CRITICAL C5800 33UF 20% 16V TANT CASE-T 128S00009 — CRITICAL C5801 33UF 20% 16V TANT CASE-T 128S00009 — C5804 2.2UF 20% 25V X6S-CERM 0402 138S00042 — C5805 2.2UF 20% 25V X6S-CERM 0402 138S00042 (MIRROR_WITH=C5804)

P3V8AON_VSW1

CRITICAL L5800 1UH-20%-11A-0.01270HM PIHA052D-SM 152S00265 — PP3V8AON_PH1

107S00373 R5800 0.004 1% 1/3W MF 0306 NO_XNET_CONNECTION=1

ICCMAX = 30 A

CRITICAL C5890 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067 — CRITICAL C5891 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067 — CRITICAL C5892 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067 — CRITICAL C5893 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067 — CRITICAL C5894 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067 — CRITICAL C5895 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067 — PP3V8_AON_VDDMAIN

MIRROR_WITH=C5887 C5886 2.2UF 20% 25V X6S-CERM 0402 138S00042 — C5887 2.2UF 20% 25V X6S-CERM 0402 138S00042 — MIRROR_WITH=C5889 C5888 2.2UF 20% 25V X6S-CERM 0402 138S00042 — C5889 2.2UF 20% 25V X6S-CERM 0402 138S00042

116S0007 R5809 1.5 5% 1/16W MF-LF 402 — P3V8AON_SNUB1 — 131S0514 C5809 150PF 5% 50V C0G-CERM 0402 <RDAR://59524111>

NOSTUFF C5814 220PF 5% 50V C0G 0201-1 — C5810 5600PF 10% 10V CERM-X7R 0201 132S0370 (NO_XNET_CONNECTION=1) — R5801 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS1_P

NOSTUFF C5815 220PF 5% 50V C0G 0201-1 — R5802 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS1_N

P3V8AON_ISEN1_P

P3V8AON_ISEN1_N

PPBUS_AON

P3V8AON_DRVH2 — R5824 1.5 5% 1/16W TK 0402 107S00371 — P3V8AON_DRVH2_R

P3V8AON_BST2 — R5823 0 5% 1/16W MTL-FILM 0402 116S0006 — P3V8AON_BST2_RC — C5831 0.22UF 10% 25V X7R 0402 132S0401 — P3V8AON_SW2

NOSTUFF D5820 SBR1A30T5 SOD523 3715S0245 3V8_EXT_DIODE — P3V8AON_PVCC

P3V8AON_DRVL2 — R5825 0.100 1% 1/4W MF 0402 104S0050 — P3V8AON_DRVL2_R — R5826 0.100 1% 1/4W MF 0402 104S0050 — P3V8AON_DRVL2_RR

ALLOW_APPLE_PREFIX=Q CRITICAL Q5820 AONE36196 DFN 376S00281 (G1, D2/S1, G2, D1, D1, VER-1)

CRITICAL C5820 33UF 20% 16V TANT CASE-T 128S00009 — CRITICAL C5821 33UF 20% 16V TANT CASE-T 128S00009 — C5824 2.2UF 20% 25V X6S-CERM 0402 138S00042 — C5825 2.2UF 20% 25V X6S-CERM 0402 138S00042 (MIRROR_WITH=C5824)

SAME SW NET ON BOTH SIDES — P3V8AON_SW2

CRITICAL L5820 0.56UH-20%-22.0A-0.00670HM PILA062D-SM-COMBO 152S01248 — PP3V8AON_PH2

107S00090 R5820 0.001 1% 1/3W MF 0306 NO_XNET_CONNECTION=1

R5829 2.2 5% 1/16W MF-LF 402 (DIDT=TRUE, SWITCH_NODE=TRUE) — P3V8AON_SNUB2 — C5829 100PF 5% 50V C0G 0402 NOSTUFF

NOSTUFF C5834 220PF 5% 50V C0G 0201-1 — C5830 5600PF 10% 10V CERM-X7R 0201 132S0370 (NO_XNET_CONNECTION=1) — R5821 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS2_P

NOSTUFF C5835 220PF 5% 50V C0G 0201-1 — R5822 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS2_N

P3V8AON_ISEN2_P

P3V8AON_ISEN2_N

PPBUS_AON

P3V8AON_DRVH3 — R5844 1.5 5% 1/16W TK 0402 107S00371 — P3V8AON_DRVH3_R

P3V8AON_BST3 — R5843 0 5% 1/16W MTL-FILM 0402 116S0006 — P3V8AON_BST3_RC — C5851 0.22UF 10% 25V X7R 0402 132S0401 — P3V8AON_SW3

NOSTUFF D5840 SBR1A30T5 SOD523 3715S0245 3V8_EXT_DIODE — P3V8AON_PVCC

P3V8AON_DRVL3 — R5845 0.100 1% 1/4W MF 0402 104S0050 — P3V8AON_DRVL3_R — R5846 0.100 1% 1/4W MF 0402 104S0050 — P3V8AON_DRVL3_RR

ALLOW_APPLE_PREFIX=Q CRITICAL Q5840 AONE36196 DFN 376S00281 (G1, D2/S1, G2, D1, D1, VER-1)

CRITICAL C5840 33UF 20% 16V TANT CASE-T 128S00009 — CRITICAL C5841 33UF 20% 16V TANT CASE-T 128S00009 — C5844 2.2UF 20% 25V X6S-CERM 0402 138S00042 — C5845 2.2UF 20% 25V X6S-CERM 0402 138S00042 (MIRROR_WITH=C5844)

SAME SW NET ON BOTH SIDES — P3V8AON_SW3

CRITICAL L5840 0.56UH-20%-22.0A-0.00670HM PILA062D-SM-COMBO 152S01248 — PP3V8AON_PH3

107S00090 R5840 0.001 1% 1/3W MF 0306 NO_XNET_CONNECTION=1

R5849 2.2 5% 1/16W MF-LF 402 (DIDT=TRUE, SWITCH_NODE=TRUE) — P3V8AON_SNUB3 — C5849 100PF 5% 50V C0G 0402 NOSTUFF

NOSTUFF C5854 220PF 5% 50V C0G 0201-1 — C5850 5600PF 10% 10V CERM-X7R 0201 132S0370 (NO_XNET_CONNECTION=1) — R5841 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS3_P

NOSTUFF C5855 220PF 5% 50V C0G 0201-1 — R5842 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS3_N

P3V8AON_ISEN3_P

P3V8AON_ISEN3_N

NO_XNET_CONNECTION=1 XW5870 SM — P3V8AON_VSNS_XW_P

NO_XNET_CONNECTION=1 XW5871 SM — P3V8AON_VSNS_XW_N

NO_XNET_CONNECTION=1 R5870 0 5% 1/20W MF 0201 117S0201 — P3V8AON_VSENSE

NOSTUFF C5870 1UF 20% 10V X6S-CERM 0201 138S00044 (NO_XNET_CONNECTION=1)

NO_XNET_CONNECTION=1 R5871 0 5% 1/20W MF 0201 117S0201 — P3V8AON_VRTN

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=ref_vr_iceman SYNC_DATE=04/20/2020

PAGE TITLE: POWER: 3V8 AON (2/2)

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DRAWING NUMBER 051-05392 SIZE D

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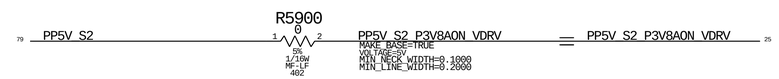
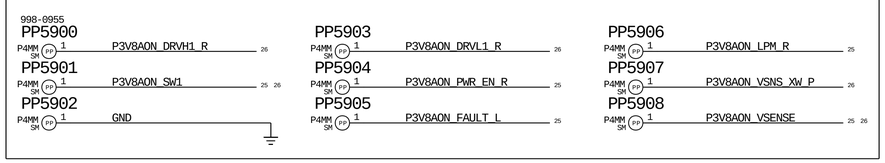
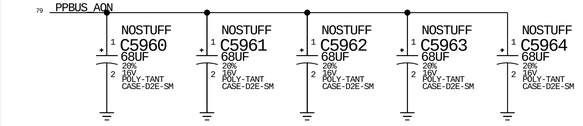
A PP5V_S2 to PP3V8_AON VDRV Connection



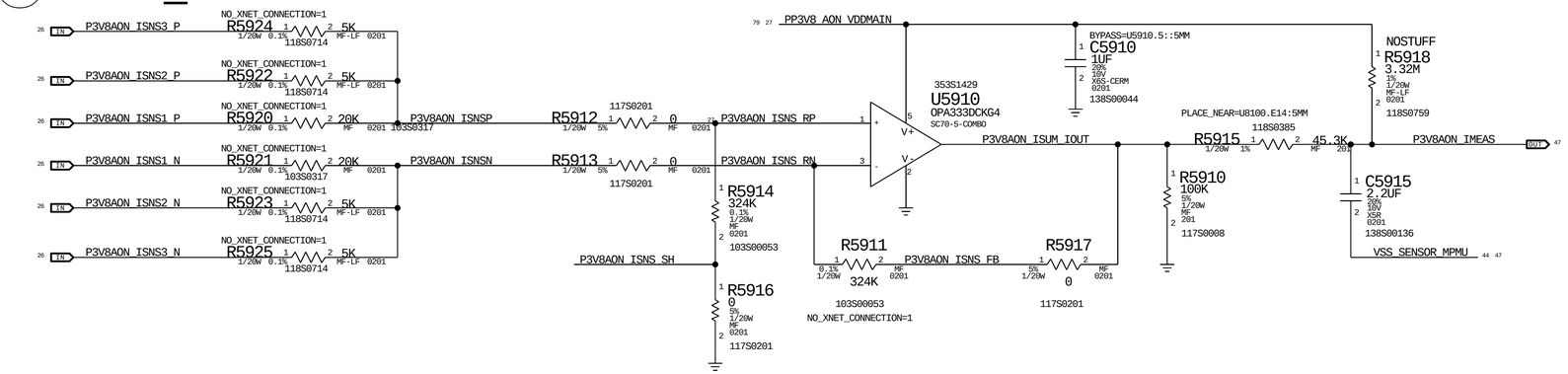
B PP3V8_AON Probe Points



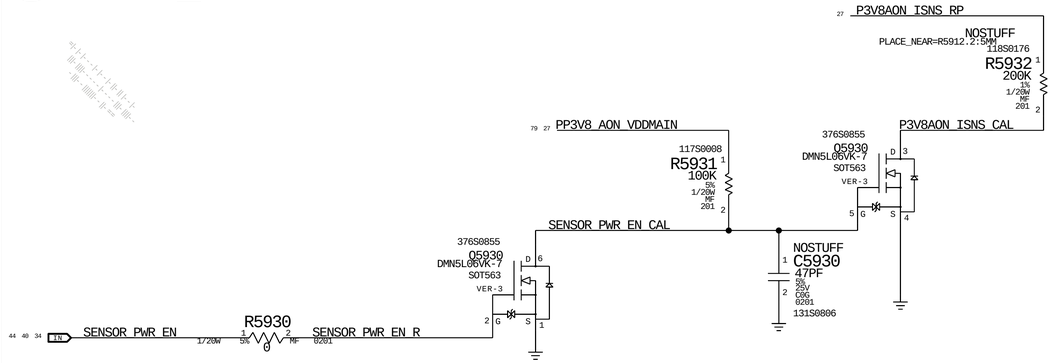
C PPBUS_AON Bulk Capacitance



D PP3V8_AON Current Sense



E PP3V8_AON Current Sense Cal Control Circuit



$X1757GHUB/mlb/sim/ltspice/pp3v8_aon_vddmain/pp3v8_aon_vddmain_current_sense.asc

SYNC_MASTER=T585_REF_VR_ICEMAN_0.36.0 SYNC_DATE=10/11/2019

PAGE TITLE
POWER: 3V8 AON SUPPORT

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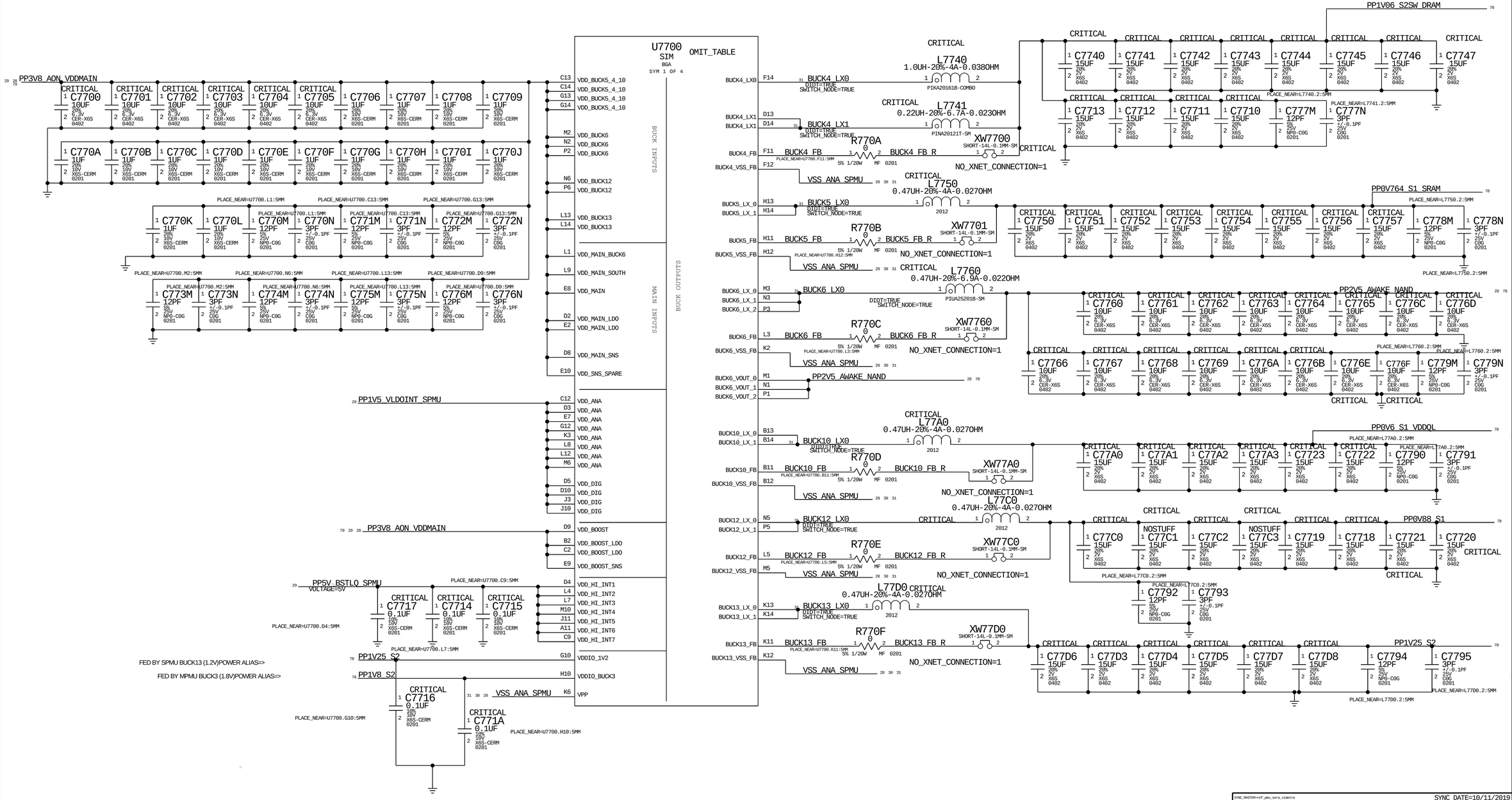
BOM_COST_GROUP=PLATFORM POWER

2 1

SLAVE PMU BUCKS



SYNC_MASTER=ref_pmu_sera_simetra	SYNC_DATE=10/11/2019
PAGE TITLE	PMU: SLAVE INPUT PWR & BUCKS
Apple Inc.	DRAWING NUMBER 051-05392 · SIZE D
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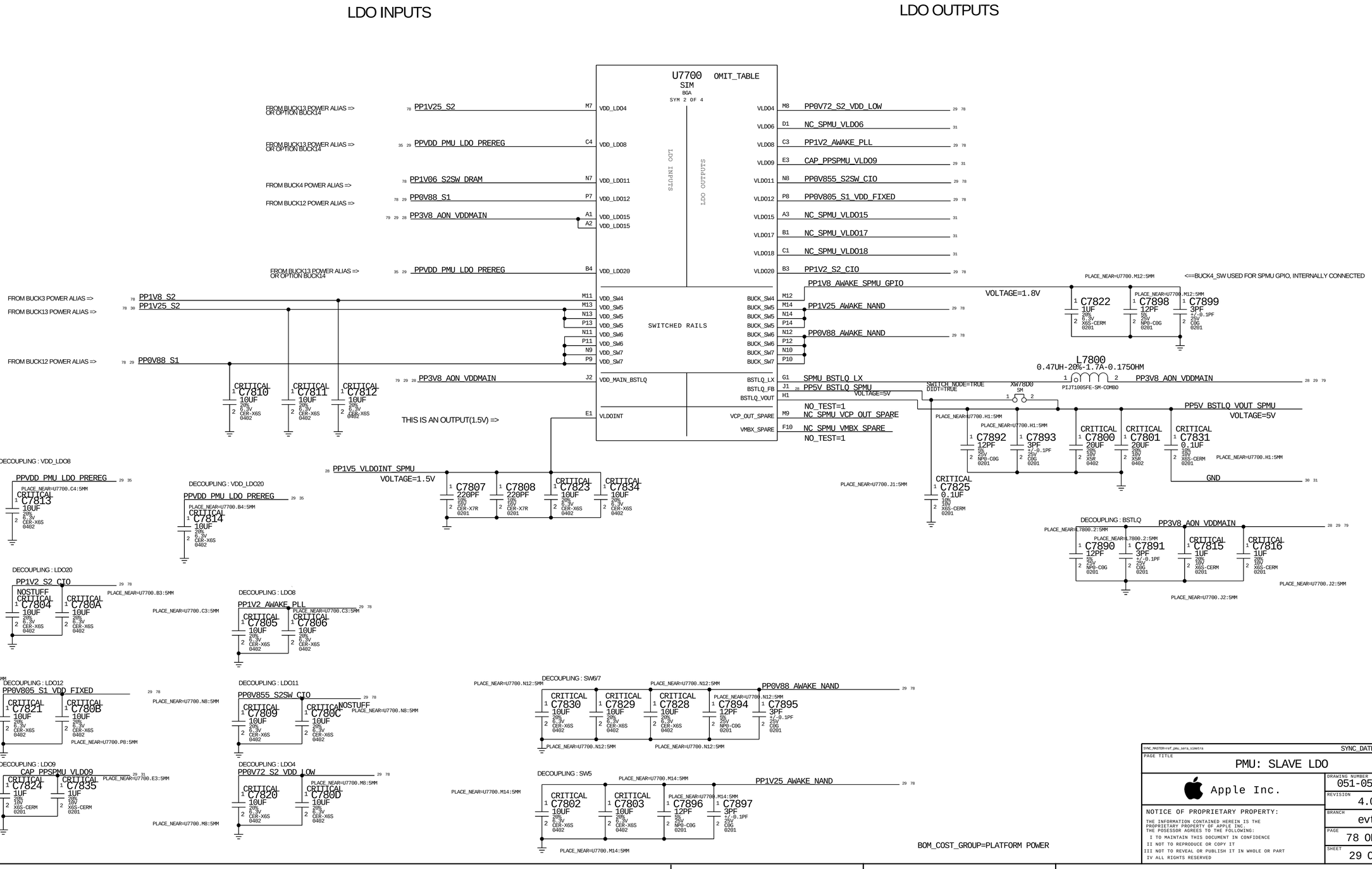
SLAVE PMU LDO



SYNC_MASTER=ref_pmu_sera_simetra SYNC_DATE=10/11/2019

PAGE TITLE
PMU: SLAVE LDO

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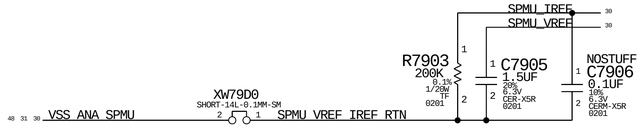
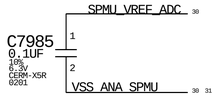
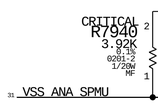
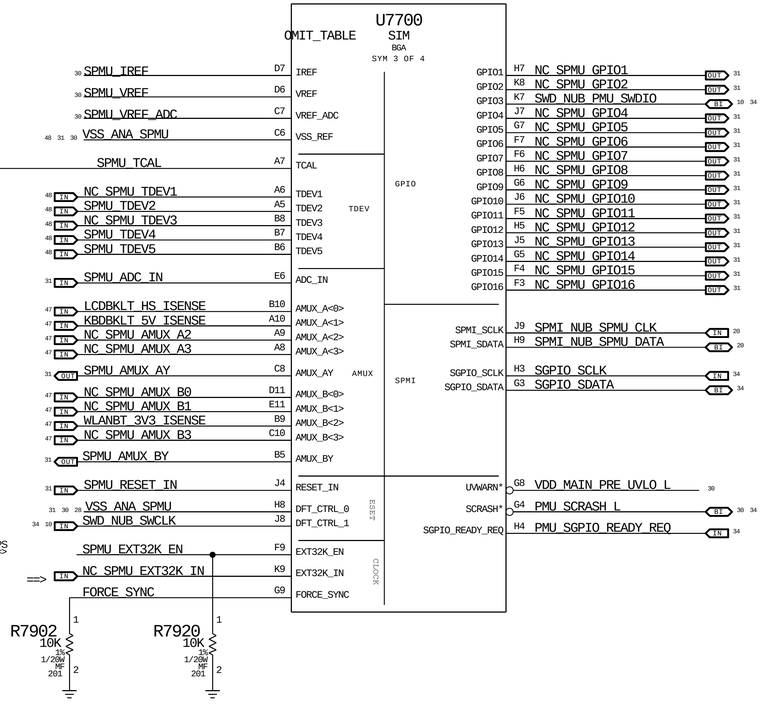
SLAVE PMU GND,ADC,& GPIO





PLACEMENT NOTE:
CONNECT VSS_REF THROUGH ALL GND PLANES PLACE XW AT VSS_REF PIN, ROUTE VSS_RTN
BACK FROM THE VREF / IREF PASSIVES



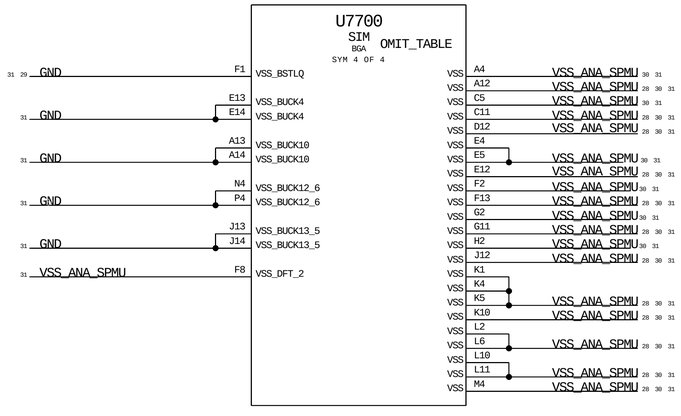


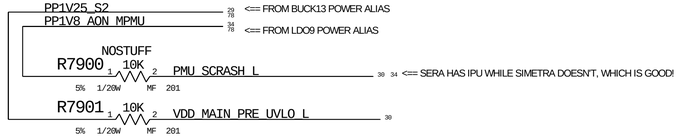
RECOMMENDED TO HAVE PD ON UNUSED RESET_IN PIN

DFT_CTRL0=0 ==> DFT_CTRL1=SWDCLK

CAN DIRECTLY SHORT TO GND BUT PD HELPS IF NEED TO OVERRIDE BY NOSTUFFING IT ==>

CAN LEAVE IT FLOATING AS OTP DISABLES IT AND HAS IBX PAD KEEPS PD ON DEV TO BE ABLE TO OVERRIDE IT





BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=vf_pmu_serra_simetra SYNC_DATE=10/11/2019

PAGE TITLE
PMU: SLAVE GPIO & GND

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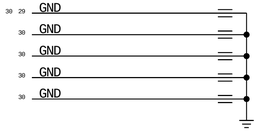
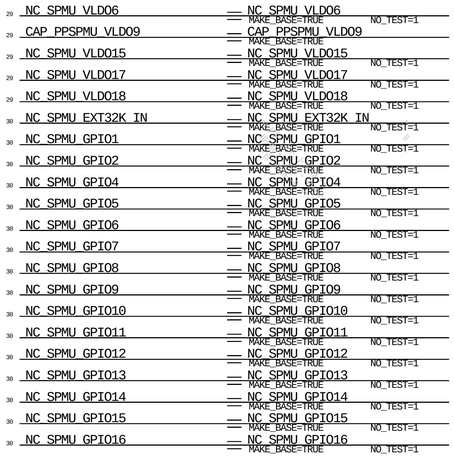
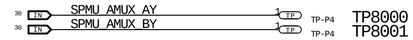
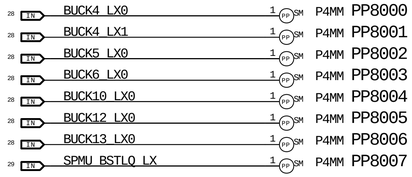
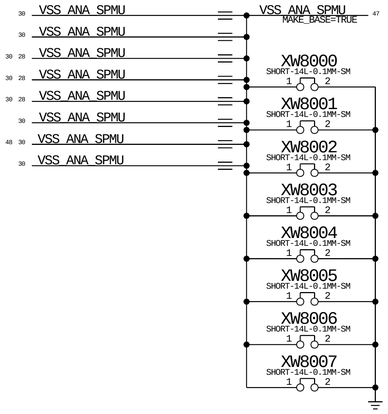
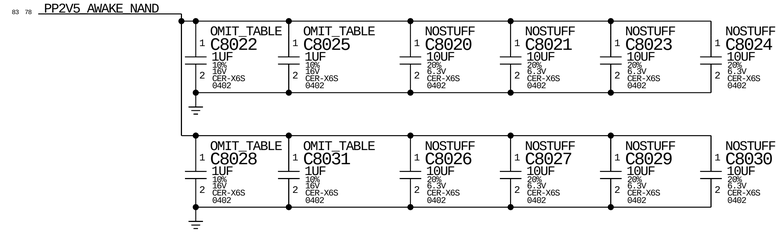




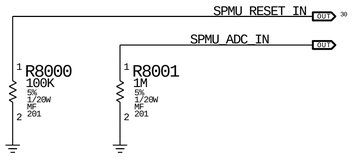








PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138s00336	5	CAP,CER,1UF,10%,16V,X6S,MLR,0402	C5151,C8022,C8025,C8028,C8031		



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=ref_pmu_sera_simetra SYNC_DATE=10/11/2019

PAGE TITLE

PMU: Slave extra

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MASTER PMU BUCKS

PP3V8_AON_VDDMAIN

C81F8 C81F9 C81E0 C81E1 C81C0 C81C1 C81C2 C81C3 C81C4 — 1UF 20% 10V X6S-CERM 0201

C81F6 C81F7 C81C6 C81C7 C81C8 C81C9 C81CA C81CB C81CC C81CD — 1UF 20% 10V X6S-CERM 0201

CRITICAL C81D0 C81D1 C81D2 C81D3 C81D4 C81D5 C81D6 C81D7 C81D8 — 10UF 20% 6.3V CER-X6S 0402

CRITICAL C81D9 C81DA C81DB C81DC C81DD C81F2 C81F3 C81F4 C81F5 — 10UF 20% 6.3V CER-X6S 0402

PLACE_NEAR=U8100.L1:5MM PLACE_NEAR=U8100.R1:5MM PLACE_NEAR=U8100.W1:5MM PLACE_NEAR=U8100.Y7:5MM

C81FJ C81FK C81FL C81FM C81FN C81FP C81FQ C81FR — 12PF 5% 25V NP0-C0G 0201 / 3PF +/-0.1PF 25V C0G 0201

PLACE_NEAR=U8100.B1:5MM PLACE_NEAR=U8100.F1:5MM PLACE_NEAR=U8100.K1:5MM PLACE_NEAR=U8100.A15:5MM

C81FA C81FB C81FC C81FD C81FE C81FF C81FG C81FH — 12PF 5% 25V NP0-C0G 0201 / 3PF +/-0.1PF 25V C0G 0201

PLACE_NEAR=U8100.B15:5MM

C81F0 12PF 5% 25V NP0-C0G 0201; C81F1 3PF +/-0.1PF 25V C0G 0201

FROM BUCK13 POWER ALIAS =>
OPTION BUCK14

PPVDD_PMU_LDO_PREREG

PP1V5_VLDOINT_MPMU

C8130 10UF 20% 6.3V CER-X6S 0402

PMU_VDD_HI

FED BY SPMU BUCK13 (1.2V)POWER ALIAS=> PP1V25_S2

FED BY MPMU BUCK3 (1.8V)POWER ALIAS=> PP1V8_S2

PLACE_NEAR=U8100.R16:5MM

CRITICAL C8131 0.1UF 10% 10V X6S-CERM 0201; CRITICAL C8132 0.1UF 10% 10V X6S-CERM 0201

COINCELL BATTERY => PP3V8_AON_VDDMAIN

PLACE_NEAR=U8100.N16:5MM

PP3V8_AON_VDDMAIN

PLACE_NEAR=U8110.5:5MM C8128 0.1UF 10% 6.3V CERM-X5R 0201

OMIT_TABLE R8100 887K 0.1% 1/20W TF 0201

PPBUS_AON — MPMU_SNS_DIV

R8101 453K 1% 1/20W MF 201 OMIT_TABLE

U8110 OPA333DCKG4 SC70-5-COMBO

PMU_VDD_HI

U8100 SER BGA SYM 1 OF 6 — OMIT_TABLE

VOLTAGE INPUTS / BUCK OUTPUTS / SENSE

L1	VDD_BUCK0_2_7_11
L2	VDD_BUCK0_2_7_11
L3	VDD_BUCK0_2_7_11
L4	VDD_BUCK0_2_7_11
R1	VDD_BUCK0_2_7_11
R2	VDD_BUCK0_2_7_11
R3	VDD_BUCK0_2_7_11
R4	VDD_BUCK0_2_7_11
W1	VDD_BUCK0_2_7_11
W2	VDD_BUCK0_2_7_11
W3	VDD_BUCK0_2_7_11
W4	VDD_BUCK0_2_7_11
W7	VDD_BUCK0_2_7_11
W11	VDD_BUCK0_2_7_11
W15	VDD_BUCK0_2_7_11
W19	VDD_BUCK0_2_7_11
Y7	VDD_BUCK0_2_7_11
Y11	VDD_BUCK0_2_7_11
Y15	VDD_BUCK0_2_7_11
Y19	VDD_BUCK0_2_7_11
A7	VDD_BUCK1_8_9
A11	VDD_BUCK1_8_9
B1	VDD_BUCK1_8_9
B2	VDD_BUCK1_8_9
B3	VDD_BUCK1_8_9
B4	VDD_BUCK1_8_9
B7	VDD_BUCK1_8_9
B11	VDD_BUCK1_8_9
F1	VDD_BUCK1_8_9
F2	VDD_BUCK1_8_9
F3	VDD_BUCK1_8_9
F4	VDD_BUCK1_8_9
K1	VDD_BUCK1_8_9
K2	VDD_BUCK1_8_9
K3	VDD_BUCK1_8_9
K4	VDD_BUCK1_8_9
A15	VDD_BUCK3_14
B15	VDD_BUCK3_14
K19	VDD_LDO2
L20	VDD_LDO3_14
K21	VDD_LDO5
J19	VDD_LDO19
C18	VDD_MAIN_WBOOST
F20	VDD_MAIN_WBOOST
F15	VDD_MAIN_WIDAC
K11	VDD_MAIN
V17	VDD_MAIN1
E19	VDD_MAIN_DRV
K10	VDD_MAIN_SNS
F19	VDD_MAIN_SNS_WLED
H8	VDD_BOOST_SNS
R16	VDDIO_1V2
N16	VDDIO_BUCK3
N20	VDD_RTC_ALT
K6	VPP

PMU_VDD_HI

VSS_ANA_MPMU

CRITICAL L8100 1.0UH-20%-4A-0.038OHM PIKA20161B-COMBO

BUCK0_LX0 (W6, Y6) — DIDT=TRUE, SWITCH_NODE=TRUE

CRITICAL L8101 0.1UH-20%-10.3A-0.010HM PCCE20161B-SM 152S01268

BUCK0_LX1 (V1, V2, V3, V4) — DIDT=TRUE, SWITCH_NODE=TRUE

BUCK0_LX2 (P1, P2, P3, P4) — DIDT=TRUE, SWITCH_NODE=TRUE

CRITICAL L8102 0.1UH-20%-10.3A-0.010HM PCCE20161B-SM 152S01268

BUCK0_LX3 (T1, T2, T3, T4) — DIDT=TRUE, SWITCH_NODE=TRUE

BUCK0_LX4 (M1, M2, M3, M4) — DIDT=TRUE, SWITCH_NODE=TRUE

BUCK0_FB (U6) — R810A 0 5% 1/20W MF 0201 — BUCK0_FB_R — XW8100 SHORT-14L-0.1MM-SM

PLACE_NEAR=U8100.U6:5MM

BUCK0_VSS_FB (T6) — VSS_ANA_MPMU

NO_XNET_CONNECTION=1

CRITICAL L8110 1.0UH-20%-4A-0.038OHM PIKA20161B-COMBO

BUCK1_LX0 (A6, B6) — DIDT=TRUE, SWITCH_NODE=TRUE

CRITICAL L8111 0.1UH-20%-10.3A-0.010HM PCCE20161B-SM 152S01268

BUCK1_LX1 (C1, C2, C3, C4) — DIDT=TRUE, SWITCH_NODE=TRUE

BUCK1_LX2 (G1, G2, G3, G4) — DIDT=TRUE, SWITCH_NODE=TRUE

CRITICAL L8112 0.1UH-20%-10.3A-0.010HM PCCE20161B-SM 152S01268

BUCK1_LX3 (E1, E2, E3, E4) — DIDT=TRUE, SWITCH_NODE=TRUE

BUCK1_LX4 (J1, J2, J3, J4) — DIDT=TRUE, SWITCH_NODE=TRUE

BUCK1_FB (D6) — R810B 0 5% 1/20W MF 0201 — BUCK1_FB_R — XW8110 SHORT-14L-0.1MM-SM

PLACE_NEAR=U8100.D6:5MM

BUCK1_VSS_FB (E6) — VSS_ANA_MPMU

NO_XNET_CONNECTION=1

CRITICAL L8120 1.0UH-20%-4A-0.038OHM PIKA20161B-COMBO

BUCK2_LX0 (Y20) — DIDT=TRUE, SWITCH_NODE=TRUE

CRITICAL L8121 0.1UH-20%-10.3A-0.010HM PCCE20161B-SM 152S01268

BUCK2_LX1 (W18, Y18) — DIDT=TRUE, SWITCH_NODE=TRUE

BUCK2_LX2 (W16, Y16) — DIDT=TRUE, SWITCH_NODE=TRUE

BUCK2_FB (V20) — R810C 0 1/20W MF 0201 — BUCK2_FB_R — XW8120 SHORT-14L-0.1MM-SM

PLACE_NEAR=U8100.V20:5MM

BUCK2_VSS_FB (U20) — VSS_ANA_MPMU

NO_XNET_CONNECTION=1

PPVDD_PCPU_AWAKE

CRITICAL C8100 C8101 C8102 C8103 C8104 C8105 — 15UF 20% 2V X6S 0402

CRITICAL C8109 C810A C810B C810C C810D C810E — 15UF 20% 2V X6S 0402

PLACE_NEAR=L8100.2:5MM PLACE_NEAR=L8101.3:5MM

C81H0 C81H1 C81H2 C81H3 — 12PF 5% 25V NP0-C0G 0201 / 3PF +/-0.1PF 25V C0G 0201

PPVDD_GPU_AWAKE

CRITICAL C8110 C8111 C8112 C8113 C8114 C8115 C811D C811E — 15UF 20% 2V X6S 0402

CRITICAL C8119 C811A C811B C811C C8116 C8117 — 15UF 20% 2V X6S 0402

PLACE_NEAR=L8110.2:5MM PLACE_NEAR=L8111.3:5MM

C81H4 C81H5 C81H6 C81H7 — 12PF 5% 25V NP0-C0G 0201 / 3PF +/-0.1PF 25V C0G 0201

PPVDD_SOC_S1

CRITICAL C8120 C8121 C8122 C8123 C8124 C8125 C8126 C8127 — 15UF 20% 2V X6S 0402

PLACE_NEAR=L8120.2:5MM

C81H8 C81H9 — 12PF 5% 25V NP0-C0G 0201 / 3PF +/-0.1PF 25V C0G 0201

BOM_COST_GROUP=PLATFORM POWER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
103S00385	1	RES,TK,887KOHM,0.1%,1/20W,0201	R8100	CRITICAL	PBUS_3S	<== FOR 3S BATTERY
103S00480	1	RES,MF,453KOHM,0.1,1/20W,0201	R8101	CRITICAL	PBUS_3S	
103S00481	1	RES,MF,910KOHM,0.1,1/20W,0201	R8100	CRITICAL	PBUS_12VDCIN	<== FOR 12V DCIN
103S00043	1	RES,MF,280KOHM,0.1,1/20W,0201	R8101	CRITICAL	PBUS_12VDCIN	
103S00385	1	RES,TK,887KOHM,0.1%,1/20W,0201	R8100	CRITICAL	PBUS_15P8VDCIN	<== FOR 15.8V DCIN
103S00086	1	RES,MF,205KOHM,0.1%,1/20W,0201	R8101	CRITICAL	PBUS_15P8VDCIN	

SYNC_MASTER=ref_pmu_sera_simetra — SYNC_DATE=10/11/2019

PAGE TITLE: PMU: MASTER INPUT PWR & BUCKS

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MASTER PMU BUCKS & GND

U8100 SER BGA SYM 6 OF 6 — OMIT_TABLE

	N1	VSS_BUCK0	VSS	A18	VSS_ANA_MPMU
	N2	VSS_BUCK0	VSS	B8	VSS_ANA_MPMU
	N3	VSS_BUCK0	VSS	B18	VSS_ANA_MPMU
	N4	VSS_BUCK0	VSS	C5	
	U1	VSS_BUCK0	VSS	C6	VSS_ANA_MPMU
	U2	VSS_BUCK0	VSS	C9	
	U3	VSS_BUCK0	VSS	C10	
	U4	VSS_BUCK0	VSS	C13	VSS_ANA_MPMU
	W5	VSS_BUCK0	VSS	C17	VSS_ANA_MPMU
	Y1	VSS_BUCK0	VSS	D5	
	Y2	VSS_BUCK0	VSS	D7	VSS_ANA_MPMU
	Y3	VSS_BUCK0	VSS	D10	
	Y4	VSS_BUCK0	VSS	D11	
GND	Y5	VSS_BUCK0	VSS	D15	VSS_ANA_MPMU
	A1	VSS_BUCK1	VSS	D18	
	A2	VSS_BUCK1	VSS	D19	
	A3	VSS_BUCK1	VSS	D20	VSS_ANA_MPMU
	A4	VSS_BUCK1	VSS	E5	
	A5	VSS_BUCK1	VSS	E7	VSS_ANA_MPMU
	B5	VSS_BUCK1	VSS	E15	VSS_ANA_MPMU
	D1	VSS_BUCK1	VSS	E17	
	D2	VSS_BUCK1	VSS	E20	VSS_ANA_MPMU
	D3	VSS_BUCK1	VSS	F6	VSS_ANA_MPMU
	D4	VSS_BUCK1	VSS	F16	
	H1	VSS_BUCK1	VSS	F17	
	H2	VSS_BUCK1	VSS	F21	
	H3	VSS_BUCK1	VSS	F22	VSS_ANA_MPMU
GND	H4	VSS_BUCK1	VSS	G5	
	W17	VSS_BUCK2	VSS	G6	VSS_ANA_MPMU
	W21	VSS_BUCK2	VSS	G15	
	W22	VSS_BUCK2	VSS	G18	VSS_ANA_MPMU
	Y17	VSS_BUCK2	VSS	H5	
	Y21	VSS_BUCK2	VSS	H6	VSS_ANA_MPMU
GND	Y22	VSS_BUCK2	VSS	H15	
	A17	VSS_BUCK3	VSS	H18	VSS_ANA_MPMU
GND	B17	VSS_BUCK3	VSS	J5	
	W13	VSS_BUCK7	VSS	J6	VSS_ANA_MPMU
GND	Y13	VSS_BUCK7	VSS	J13	VSS_ANA_MPMU
	A9	VSS_BUCK8	VSS	J17	
GND	B9	VSS_BUCK8	VSS	J18	
	A13	VSS_BUCK9_14	VSS	K15	
GND	B13	VSS_BUCK9_14	VSS	K18	VSS_ANA_MPMU
	W9	VSS_BUCK11	VSS	L6	
GND	Y9	VSS_BUCK11	VSS	L7	VSS_ANA_MPMU
GND	V22	VSS_BSTLQ	VSS	L8	
	A21	VSS_WLED_LP	VSS	L9	
	A22	VSS_WLED_LP	VSS	L10	
	B21	VSS_WLED_LP	VSS	L11	
	B22	VSS_WLED_LP	VSS	L12	VSS_ANA_MPMU
	A20	VSS_WLED_HP1	VSS	L15	VSS_ANA_MPMU
	B20	VSS_WLED_HP1	VSS	M5	
	C20	VSS_WLED_HP1	VSS	N5	VSS_ANA_MPMU
	D21	VSS_WLED_HP2	VSS	N18	VSS_ANA_MPMU
	D22	VSS_WLED_HP2	VSS	N22	VSS_ANA_MPMU
VSS_ANA_MPMU	J11	VSS_REF	VSS	P5	
VSS_ANA_MPMU	K7	VSS_DFT_2	VSS	P7	VSS_ANA_MPMU
			VSS	R18	VSS_ANA_MPMU
			VSS	T5	VSS_ANA_MPMU
			VSS	T18	VSS_ANA_MPMU
			VSS	U5	VSS_ANA_MPMU
			VSS	U19	VSS_ANA_MPMU
			VSS	V5	VSS_ANA_MPMU
			VSS	V6	
			VSS	V9	VSS_ANA_MPMU
			VSS	V10	
			VSS	V13	
			VSS	V14	
			VSS	V16	
			VSS	V18	VSS_ANA_MPMU
			VSS	V21	VSS_ANA_MPMU
			VSS	W8	
			VSS	W12	VSS_ANA_MPMU
			VSS	W20	VSS_ANA_MPMU

UNUSED ADC_IN PIN NEED 1M PD

MPMU_ADC_IN — PP1V5_VLDOINT_MPMU — PLACE_NEAR=U8100.C15:5MM — C8206 0.1UF 10% 16V X6S-CERM 0201

U8100 SER BGA SYM 2 OF 6 — OMIT_TABLE

K9	ADC_IN	
C7	VDD_ANA	
C11	VDD_ANA	
C15	VDD_ANA	
F5	VDD_ANA	
F18	VDD_ANA	
J15	VDD_ANA	
K5	VDD_ANA	
K8	VDD_ANA	
L5	VDD_ANA	
P18	VDD_ANA	
R5	VDD_ANA	
V7	VDD_ANA	
V11	VDD_ANA	
V15	VDD_ANA	
V19	VDD_ANA	
D9	VDD_DIG	
E16	VDD_DIG	
J7	VDD_DIG	
M18	VDD_DIG	
P9	VDD_DIG	
R17	VDD_DIG	
K12	VREF	MPMU_VREF
J10	VBAT	MPMU_VBAT
J9	IBAT	MPMU_IBAT
J8	IREF	MPMU_IREF

UNUSED VBAT/IBAT PINS NEED 1M PD

BUCK OUTPUTS

BUCK3_LX	A16	BUCK3_LX0	DIDT=TRUE, SWITCH_NODE=TRUE
BUCK3_LX	B16		
BUCK3_FB	D16	BUCK3_FB	PLACE_NEAR=U8100.D16:5MM
BUCK3_VSS_FB	C16	VSS_ANA_MPMU	
BUCK7_LX0	Y12	BUCK7_LX0	DIDT=TRUE, SWITCH_NODE=TRUE
BUCK7_LX1	W14	BUCK7_LX1	DIDT=TRUE, SWITCH_NODE=TRUE
BUCK7_LX1	Y14		
BUCK7_FB	U12	BUCK7_FB	PLACE_NEAR=U8100.U12:5MM
BUCK7_VSS_FB	V12	VSS_ANA_MPMU	
BUCK8_LX0	A8	BUCK8_LX0	DIDT=TRUE, SWITCH_NODE=TRUE
BUCK8_LX1	A10	BUCK8_LX1	DIDT=TRUE, SWITCH_NODE=TRUE
BUCK8_LX1	B10		
BUCK8_FB	D8	BUCK8_FB	
BUCK8_VSS_FB	C8	VSS_ANA_MPMU	PLACE_NEAR=U8100.D8:5MM
BUCK9_LX	A12	BUCK9_LX0	DIDT=TRUE, SWITCH_NODE=TRUE
BUCK9_LX	B12		
BUCK9_FB	D12	BUCK9_FB	
BUCK9_VSS_FB	C12	VSS_ANA_MPMU	PLACE_NEAR=U8100.D12:5MM
BUCK11_LX0	Y8	BUCK11_LX0	DIDT=TRUE, SWITCH_NODE=TRUE
BUCK11_LX1	W10	BUCK11_LX1	DIDT=TRUE, SWITCH_NODE=TRUE
BUCK11_LX1	Y10		
BUCK11_FB	U8	BUCK11_FB	
BUCK11_VSS_FB	V8	VSS_ANA_MPMU	PLACE_NEAR=U8100.U8:5MM
BUCK14_LX	A14	BUCK14_LX0	
BUCK14_LX	B14		
BUCK14_FB	D14	BUCK14_FB	
BUCK14_VSS_FB	C14	VSS_ANA_MPMU	

L8230 CRITICAL 0.47UH-20%-4A-0.027OHM 2012 — R820A 0 5% 1/20W MF 0201 — XW8230 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1

L8270 1.0UH-20%-4A-0.038OHM PIKA20161B-COMBO — L8271 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM — R820B 0 5% 1/20W MF 0201 — XW8270 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1

L8280 1.0UH-20%-4A-0.038OHM PIKA20161B-COMBO — L8281 CRITICAL 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM — R820C 0 5% 1/20W MF 0201 — XW8280 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1

L8290 CRITICAL 0.47UH-20%-4A-0.027OHM 2012 — R820D 0 5% 1/20W MF 0201 — XW8290 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1

L82B0 CRITICAL 1.0UH-20%-4A-0.038OHM PIKA20161B-COMBO — L82B1 CRITICAL 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM — R820E 0 5% 1/20W MF 0201 — XW82B0 SHORT-14L-0.1MM-SM — NO_XNET_CONNECTION=1

VIN FROM BUCK13 IS POR FOR LDO4.20 & IF PDN (VMIN VIOLATION, WHEN LDOS IN DROPOUT MODE) IS AN ISSUE THEN BUCK14 WILL BE THE BACKUP OPTION. THIS WOULD THEN REQUIRE ADDING BEAD AND CAPS

SWITCHED RAILS

PP1V8_S2 (FROM BUCVK3 POWER ALIAS =>)	R21	VDD_SW1	
	R22	VDD_SW1	
	T20	VDD_SW2	
PP1V25_S2 (FROM BUCK13 POWER ALIAS =>)	R19	VDD_SW3	
	R20	VDD_SW3	
	P21	BUCK_SW1	PP1V8_AWAKE
	P22	BUCK_SW1	
	T19	BUCK_SW2	NC_MPMU_BUCK_SW2 (NO_TEST=1)
	P19	BUCK_SW3	
	P20	BUCK_SW3	PP1V25_AWAKE_IO

DECOUPLING : VDD_SW3

PP1V25_S2 — PLACE_NEAR=U8100.R19:5MM — CRITICAL C8201 10UF 20% 6.3V CER-X6S 0402

MPMU_VREF — MPMU_IREF — C8204 1.5UF 20% 6.3V CER-X5R 0201 — R8201 200K 0.1% 1/20W TF 0201 — NOSTUFF C8205 0.1UF 10% 6.3V CERM-X5R 0201

XW82B2 SHORT-14L-0.1MM-SM — VSS_ANA_MPMU — MPMU_VREF_IREF_RTN

PLACEMENT NOTE:
CONNECT VSS_REF THROUGH ALL GND PLANES PLACE XW AT VSS_REF PIN, ROUTE VSS_RTN BACK FROM THE VREF / IREF PASSIVES

CRITICAL C8240 15UF 20% 6.3V X6S 0402 — CRITICAL C8241 15UF 20% 6.3V X6S 0402 — PP1V25_AWAKE_IO

CRITICAL C8202 10UF 20% 6.3V CER-X6S 0402 — CRITICAL C8203 10UF 20% 6.3V CER-X6S 0402 — PP1V8_AWAKE

PP1V8_S2: CRITICAL C8230–C8235 10UF 20% 6.3V CER-X6S 0402; C8D0 12PF 5% 25V NP0-C0G 0201; C8D1 3PF ±0.1PF 25V C0G 0201; PLACE_NEAR=L8230.1:5MM

CRITICAL C8236–C8239 10UF 20% 6.3V CER-X6S 0402; C823A 10UF 20% 6.3V CER-X6S 0402; C823B 10UF 20% 6.3V CER-X6S 0402

PPVDD_CPU_SRAM_AWAKE: CRITICAL NOSTUFF C8270–C8277 15UF 20% 2V X6S 0402; PLACE_NEAR=L8270.1:5MM; PLACE_NEAR=L8271.1:5MM; C82D2 12PF 5% 25V NP0-C0G 0201; C82D3 3PF ±0.1PF 25V C0G 0201

PPVDD_DISP_S1: CRITICAL C8280–C8285 15UF 20% 2V X6S 0402; C82D4 12PF 5% 25V NP0-C0G 0201; C82D5 3PF ±0.1PF 25V C0G 0201; PLACE_NEAR=L8280.1:5MM; PLACE_NEAR=L8281.1:5MM

PPVDD_DCS_S1: PLACE_NEAR=L8290.1:5MM; CRITICAL C8295, C8290–C8294 15UF 20% 2V X6S 0402; C82D6 12PF 5% 25V NP0-C0G 0201; C82D7 3PF ±0.1PF 25V C0G 0201

PPVDD_ECPU_AWAKE: CRITICAL C82B6–C82B9 15UF 20% 2V X6S 0402; NOSTUFF C82B1–C82B2 15UF 20% 2V X6S 0402; CRITICAL C82B3–C82B4 15UF 20% 2V X6S 0402; PLACE_NEAR=L82B0.1:5MM; PLACE_NEAR=L82B1.1:5MM; C82D8 12PF 5% 25V NP0-C0G 0201; C82D9 3PF ±0.1PF 25V C0G 0201

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: PMU: MASTER BUCKS & GND

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MASTER PMU LDO,ADC, & GPIO

U8100 SER OMIT_TABLE
BGA SYM 5 OF 6

NO_TEST=1	NC_MPMU_IDAC_OUT<0>	G17	IDAC_OUT<0>	WLED_LP_LX	C21 NC_MPMU_WLED_LP_LX_0 NO_TEST=1
NO_TEST=1	NC_MPMU_IDAC_OUT<1>	G16	IDAC_OUT<1>	WLED_LP_LX	C22 NC_MPMU_WLED_LP_LX_1 NO_TEST=1
NO_TEST=1	NC_MPMU_IDAC_OUT<2>	G14	IDAC_OUT<2>		
NO_TEST=1	NC_MPMU_IDAC_OUT<3>	G13	IDAC_OUT<3>		
NO_TEST=1	NC_MPMU_IDAC_OUT<4>	H17	IDAC_OUT<4>	WLED_HP1_LX	A19 NC_MPMU_WLED_HP1_LX_0 NO_TEST=1
NO_TEST=1	NC_MPMU_IDAC_OUT<5>	H16	IDAC_OUT<5>	WLED_HP1_LX	B19 NC_MPMU_WLED_HP1_LX_1 NO_TEST=1
NO_TEST=1	NC_MPMU_IDAC_OUT<6>	H14	IDAC_OUT<6>	WLED_HP1_LX	C19 NC_MPMU_WLED_HP1_LX_2 NO_TEST=1
NO_TEST=1	NC_MPMU_IDAC_OUT<7>	H13	IDAC_OUT<7>		
NO_TEST=1	NC_MPMU_IDAC_OUT<8>	J16	IDAC_OUT<8>		
NO_TEST=1	NC_MPMU_IDAC_OUT<9>	J14	IDAC_OUT<9>	WLED_HP2_LX	E21 NC_MPMU_WLED_HP2_LX_0 NO_TEST=1
NO_TEST=1	NC_MPMU_IDAC_OUT<10>	K17	IDAC_OUT<10>	WLED_HP2_LX	E22 NC_MPMU_WLED_HP2_LX_1 NO_TEST=1
NO_TEST=1	NC_MPMU_IDAC_OUT<11>	K16	IDAC_OUT<11>		
NO_TEST=1	NC_MPMU_IDAC_OUT<12>	K14	IDAC_OUT<12>		
NO_TEST=1	NC_MPMU_IDAC_OUT<13>	K13	IDAC_OUT<13>	WLED_VOUT_FB	E18 NC_MPMU_WLED_VOUT_FB NO_TEST=1
NO_TEST=1	NC_MPMU_IDAC_OUT<14>	L17	IDAC_OUT<14>		
NO_TEST=1	NC_MPMU_IDAC_OUT<15>	L16	IDAC_OUT<15>		
NO_TEST=1	NC_MPMU_IDAC_OUT<16>	L14	IDAC_OUT<16>	VCP_OUT_SPARE	U21 NC_MPMU_VCP_OUT_SPARE NO_TEST=1
NO_TEST=1	NC_MPMU_IDAC_OUT<17>	L13	IDAC_OUT<17>	VMBX_SPARE	J12 NC_MPMU_VMBX_SPARE NO_TEST=1

CRITICAL L8300 0.47UH-20%-1.7A-0.1750HM
PP3V8_AON_VDDMAIN — PLACE_NEAR=L8300.1:5MM — PIJT1005FE-SM-COMBO
35 MPMU_BSTLQ_LX — SWITCH_NODE=TRUE DIDT=TRUE
PP5V_BSTLQ_VOUT_MPMU — VOLTAGE=5V
35 34 32 79 PP3V8_AON_VDDMAIN — XW83D0 SM
PP5V_BSTLQ_MPMU — VOLTAGE=5V
C83A0 12PF 5% 25V NP0-C0G 0201 — C83A1 3PF +/-0.1PF 25V C0G 0201
CRITICAL C8300 20UF 20% 6.3V X5R 0402 — CRITICAL C8301 20UF 20% 6.3V X5R 0402
CRITICAL C8302 0.1UF 10% 16V X6S-CERM 0201
CRITICAL C8310 0.1UF 10% 16V X6S-CERM 0201 — CRITICAL C8311 0.1UF 10% 16V X6S-CERM 0201
CRITICAL C8316 0.1UF 10% 16V X6S-CERM 0201 — CRITICAL C8317 0.1UF 10% 16V X6S-CERM 0201
PLACE_NEAR=U8100.T21:5MM — PLACE_NEAR=U8100.L18:5MM — PLACE_NEAR=U8100.T22:5MM — PLACE_NEAR=U8100.D17:5MM — PLACE_NEAR=U8100.H12:5MM
C83A2 12PF 5% 25V NP0-C0G 0201 — C83A3 3PF +/-0.1PF 25V C0G 0201
GND — 33 35

VDD_HI_INT1 T21 — VDD_HI_INT2 H11 — VDD_HI_INT3 D13 — VDD_HI_INT4 D17 — VDD_HI_INT5 H12 — VDD_HI_INT6 L18
BSTLQ_LX — BSTLQ_VOUT T22 — VDD_BOOST H9 — VDD_SNS_SPARE H10

U8100 SER OMIT_TABLE
BGA SYM 3 OF 6

PP3V8_AON_VDDMAIN 79 35 34 32	VDD_BOOST_LDO	G19	VLDO1	J22	NC_MPMU_VLDO1 78
CRITICAL C8314 10UF 20% 6.3V CER-X6S 0402 — CRITICAL C8315 10UF 20% 6.3V CER-X6S 0402	VDD_BOOST_LDO	G21	VLDO2	K20	NC_MPMU_VLDO2 NO_TEST=1
	VDD_BOOST_LDO	H19	VLDO3	L21	PP1V2_S2 34 78
	VDD_BOOST_LDO	H21	VLDO5	K22	NC_MPMU_VLDO5 35
	VDD_BOOST_LDO	J21	VLDO7	H22	PP3V3_S2_UPC 34 78
	VDD_MAIN_LDO	M20	VLDO9	M19	PP1V8_AON_MPMU 34 78
LDO1 NOT USED ==> INT PD ENABLED			VLDO10	G20	NC_MPMU_VLDO10 35
35 NC_MPMU_LDO1_EN	LDO1_EN	N17	VLDO13	H20	NC_MPMU_VLDO13 35
THIS IS AN OUTPUT ==> 33 32 34 PP1V5_VLDOINT_MPMU VOLTAGE=1.5V	VLDOINT	M21	VLDO14	L19	NC_MPMU_VLDO14 35
THIS IS AN OUTPUT ==>	VLDORTC	N21	VLDO16	G22	NC_MPMU_VLDO16 35
			VLDO19	J20	NC_MPMU_VLDO19 NO_TEST=1
			VREF_ADC	H7	MPMU_VREF_ADC

LDO OUTPUTS

C8321 0.1UF 10% 6.3V CERM-X5R 0201
48 35 33 VSS_ANA_MPMU

PP1V2_S2 34 78
CRITICAL C8307 10UF 20% 6.3V CER-X6S 0402 — CRITICAL C830A 10UF 20% 6.3V CER-X6S 0402 — CRITICAL C8309 10UF 20% 6.3V CER-X6S 0402

PP1V5_VLDOINT_MPMU — PLACE_NEAR=U8100.M21:5MM — PLACE_NEAR=U8100.M21:5MM — 32 33 34
CRITICAL C8322 10UF 20% 6.3V CER-X6S 0402 — CRITICAL C830D 10UF 20% 6.3V CER-X6S 0402 — C830G 220PF 10% 16V CER-X7R 0201 — C830H 220PF 10% 16V CER-X7R 0201
PLACE_NEAR=U8100.M21:5MM — PLACE_NEAR=U8100.M21:5MM

PP1V8_AON_MPMU 34 78
CRITICAL C8304 1UF 20% 10V X6S-CERM 0201 — CRITICAL C830C 1UF 20% 10V X6S-CERM 0201

PP3V3_S2_UPC 34 78
NOSTUFF CRITICAL C8303 10UF 20% 6.3V CER-X6S 0402 — CRITICAL C830E 10UF 20% 6.3V CER-X6S 0402

INTEGRATOR ALIAS TO:
1V8 OCARINA=Y
1V2 OCARINA=N

PP1V25_S2 78
R8343 10K 5% 1/20W MF 201 — PMU_SYS_ALIVE 34 35 65 82
NOSTUFF

PP1V8_AON_MPMU 30 34 78 <== LDO9 POWER ALIAS
R8324 10K 5% 1/20W MF 201 — PMU_ONOFF_L 34 35 50 82
R8325 100K 5% 1/20W MF 201 — PMU_RSLOC_RST_L 34 35 77 82
R8338 100K 5% 1/20W MF 201 — NOSTUFF MPMU_FAULT_OUT_L 34
R8339 10K 5% 1/20W MF 201 — NOSTUFF PMU_CRASH_L 34
OTP HAS IPU

U8100 SER OMIT_TABLE
BGA SYM 6 OF 6

48 TDEV	NC_MPMU_TDEV1	E8	TDEV1	GPIO01	P16 IPD_LID_OPEN_1V8 IN 71 77
48 TDEV	NC_MPMU_TDEV2	F9	TDEV2	GPIO02	T9 CHGR_AUX_OK IN 24
48 TDEV	MPMU_TDEV3	F8	TDEV3	GPIO03	T7 SWD_NUB_PMU_SWDIO BI 10 30
48 TDEV	MPMU_TDEV4	F7	TDEV4	IPU GPIO04	R11 CODEC_WAKE_L IN 50 75
48 TDEV	MPMU_TDEV5	G9	TDEV5	GPIO05	T8 WLBT_WAKE IN 60 61
48 TDEV	NC_MPMU_TDEV6	G10	TDEV6	GPIO06	U7 IPD_PWR_EN IN 35 GPIO6=ENET_WAKE_L ==> DESKTOP GPIO6=IPD_PWR_EN ==> PORTABLE
48 TDEV	MPMU_TDEV7	G8	TDEV7	GPIO07	T11 NC_HDMI_CEC_IRQ IN 35 GPIO6 NEED PD ON PORTABLES
48 TDEV	MPMU_TDEV8	G7	TDEV8	GPIO08	U10 NC_USB3_WAKE IN 35 <= FOR J274 ONLY
				GPIO09	R12 NC_HDMI_RESET_L OUT 35 <= FOR DESKTOPS ONLY
	MPMU_TCAL	F10	TCAL	GPIO10	U9 LCD_PWR_EN OUT 34 35 <= FOR J274 ONLY
CRITICAL R8320 3.92K 0.1% 0201-2 1/20W MF — C8320 100PF 5% 25V C0G 0201				GPIO11	T12 P3V3S2_PWR_EN_MPMU OUT 34 35 GPIO10=P5VS2_PWR_EN ==> DESKTOP GPIO10=LCD_PWR_EN ==> PORTABLE
35 VSS_ANA_MPMU				GPIO12	U11 PVDD1_PWR_EN OUT 34 40
				GPIO13	T13 WLBT_PWR_EN OUT 34 60 61
				GPIO14	U13 IPD_WAKE_L OUT 34 35 GPIO14=ENET_PWR_EN ==> DESKTOP
				GPIO15	M13 SE_PWR_EN OUT 21 34 GPIO14=TPAD_KBD_WAKE_L ==> PORTABLE
				GPIO16	M14 SENSOR_PWR_EN OUT 27 34 40 44
				GPIO17	N14 NAND0_LPB_L OUT 62 63
				GPIO18	R13 BL_PWR_EN OUT 69 HDMI_CECFET_EN==> FOR J274 ONLY
				GPIO19	U14 P3V8AON_LPM OUT 34 35 FOR PORTABLES
				GPIO20	U15 P5VS2_PWR_EN OUT 35 GPIO20=LCD_PWR_EN ==>J456/J457
				GPIO21	T14 NC_MPMU_NAND0_RESET_L OUT 65 GPIO20=HDMI_PWR_EN ==>J274
				GPIO22	U16 IPD_OCP_FLT IN 35 GPIO20=P5VS2_PWR_EN ==>PORTABLE
				GPIO23	U17 NC_USB3_PWR_EN OUT 35 <= FOR DESKTOP ONLY
				GPIO24	R14 NC_MPMU_GPIO24 OUT 35 FOR J456 ONLY (ENABLE UWB LDO)
				GPIO25	N10 P2V5_NAND0_DISCHARGE_EN OUT 64
				GPIO26	P8 NC_FAN_PWR_EN OUT 35
				GPIO27	P17 NC_MPMU_GPIO27 OUT 35

82 50 35 34 PMU_ONOFF_L		P10	BUTTON1	BUTTON01	N7 NC_MPMU_BUTTON01 OUT <= NOT USED 35
82 77 35 34 PMU_RSLOC_RST_L		M6	BUTTON2	BUTTON02	N9 NC_MPMU_BUTTON02 OUT <= NOT USED 35
35 NC_MPMU_BUTTON3		N8	BUTTON3	BUTTON03	M7 NC_MPMU_BUTTON03 OUT <= NOT USED 35
35 NC_MPMU_BUTTON4		P11	BUTTON4	DBLCLICK_DET	N6 DBL_CLICK_DET OUT 7
10 SOC_WDOG		N11	RESET_IN1	RESET*	N13 PMU_RESET_L OUT 6 10 72 82
35 PMU_RESET_1V8		M10	RESET_IN2	1V2 OUTPUT	
7 SOC_SOCHOT_L		M9	RESET_IN3		
XW83D1 SHORT-14L-0.1MM-SM — 78 34 30 PP1V8_AON_MPMU	MPMU_VBUS_DET	R7	VBUS_DET	FORCE_DFU	T10 SOC_FORCE_DFU OUT PMOS OD 6 54 82
35 33 VSS_ANA_MPMU		E9	BRICK_ID1	FAULT_OUT*	M12 MPMU_FAULT_OUT_L 34
		E10	BRICK_ID2	SCRASH*	N12 PMU_SCRASH_L BI 30
PMU_SHDN		M8	SHDN IPD	SGPIO_READY_REQ	M15 PMU_SGPIO_READY_REQ OUT 30
R8322 10K 1% 1/20W MF 201 — NOSTUFF				SGPIO_SCLK	N15 SGPIO_SCLK_R 34
				SGPIO_SDATA	P15 SGPIO_SDATA_R 34
				SPMI_SCLK	R15 SPMI_NUB_MPMU_CLK IN 20
				SPMI_SDATA	T15 SPMI_NUB_MPMU_DATA BI 20
35 33 32 VSS_ANA_MPMU		N19	NXTAL_MEMS	SLEEP_32K	U18 PMU_CLK32K_SOC_R 1 R8331 33 2 PMU_CLK32K_SOC OUT 10 5% 1/20W MF 201
34 MPMU_XIN		L22	XIN	OUT_32K	T16 PMU_CLK32K_WLBT_R 1 R8330 33 2 PMU_CLK32K_WLBT OUT 60 61
34 MPMU_XOUT		M22	XOUT		PLACE_NEAR=U8100.T16:5MM 5% 1/20W MF 201
NXTAL_MEMS=0 ==> XTAL				CRASH*	P12 PMU_CRASH_L 34
47 DCIN_VSENSE		E13	AMUX_A<0>	DFT_CTRL0	M16 VSS_ANA_MPMU 33 35
47 DCIN_ISENSE		F11	AMUX_A<1>	DFT_CTRL1	M17 SWD_NUB_SWCLK IN 10 30
47 PBUS_VSENSE		E12	AMUX_A<2>	SYS_ALIVE	M11 PMU_SYS_ALIVE OUT 34 35 65 82
47 BMON_ISENSE		E11	AMUX_A<3>	ACTIVE_READY	P13 PMU_ACTIVE_READY OUT 6 53 82
35 MPMU_AMUX_AY		G12	AMUX_AY	REQUEST_DFU	R6 MPMU_REQUEST_DFU 34
47 P3V8AON_IMEAS		E14	AMUX_B<0>	CPU_TRIGGER0*	P6 BUCK0_THERMAL_THROTTLE_L OD OUT 7 35
47 P3V3S2_HS_ISENSE		F14	AMUX_B<1>	CPU_TRIGGER1*	R9 PMU_VDDHI_UVWARN_L OD OUT <= TO SOC ON PORTABLES ONLY
47 P5VS2_HS_ISENSE		F12	AMUX_B<2>	GPU_TRIGGER0*	R8 BUCK1_THERMAL_THROTTLE_L OD OUT 7 35
47 NC_MPMU_AMUX_B3		F13	AMUX_B<3>	GPU_TRIGGER1*	R10 NC_GPU_TRIGGER1_L OD OUT 35
35 MPMU_AMUX_BY		G11	AMUX_BY	UVWARN*	P14 PMU_VDDMAIN_UVWARN_L OD OUT 7 35
				VDD_BOOST_UVLO*	T17 TPT_MPMU_BOOST_UVLO_L OD OUT 35

TDEV GPIO BUTTONS RESET SPMI CLOCKS AMUX THROTTLE
MPMU BOOST UVLO IS OD, IF NEED TO PROBE OR USE IT , ADD A PU
INTERNAL PULL CAN BE ENABLED AS WELL!

NOSTUFF
R8326 100K 5% 1/20W MF 201 — WLBT_PWR_EN 34 60 61
R8327 100K 5% 1/20W MF 201 — NOSTUFF SE_PWR_EN 21 34
R8328 100K 5% 1/20W MF 201 — NOSTUFF LCD_PWR_EN 34 35
R8329 100K 5% 1/20W MF 201 — P3V3S2_PWR_EN_MPMU 34 35
R8335 100K 5% 1/20W MF 201 — SENSOR_PWR_EN 27 34 40 44
R8336 100K 5% 1/20W MF 201 — NOSTUFF IPD_WAKE_L 34 35
117S0008

R8334 10K 5% 1/20W MF 201 — MPMU_REQUEST_DFU 34
R8337 100K 5% 1/20W MF 201 — P3V8AON_LPM 34 35
R8344 100K 5% 1/20W MF 201 — NOSTUFF PVDD1_PWR_EN 34 40

R8313 0 1/20W 5% MF 0201
MPMU_XTAL1_R — MPMU_XOUT 34
MPMU_XIN 34
CRITICAL Y8301 32.768KHZ-20PPM-12.5PF 1.60X1.00-SM — NOSTUFF R8318 1M 5% 1/20W MF 201
CRITICAL C8312 18PF 5% 25V C0G-CERM 0201 — CRITICAL C8313 18PF 5% 25V C0G-CERM 0201
VSS_ANA_MPMU 33 35
INTERNAL XTAL DRIVER CIRCUIT IS CONNECTED TO CLOSEST VSS PIN N22

34 SGPIO_SCLK_R — PLACE_NEAR=U8100.N15:5MM — R8341 20 5% 1/20W MF 201 — SGPIO_SCLK OUT 30
34 SGPIO_SDATA_R — PLACE_NEAR=U8100.P15:5MM — R8342 20 5% 1/20W MF — SGPIO_SDATA OUT 30

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=ref_pmu_sara_518473a — SYNC_DATE=04/28/2010

PAGE TITLE
PMU: MASTER LDO & GPIO

Apple Inc.

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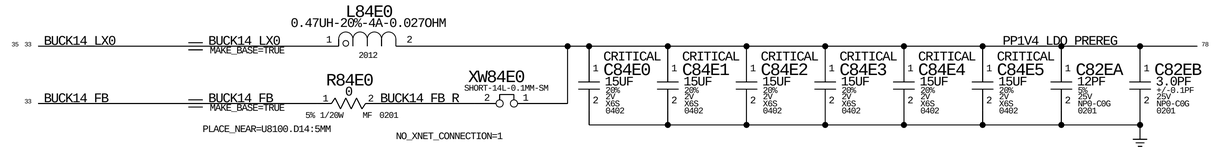
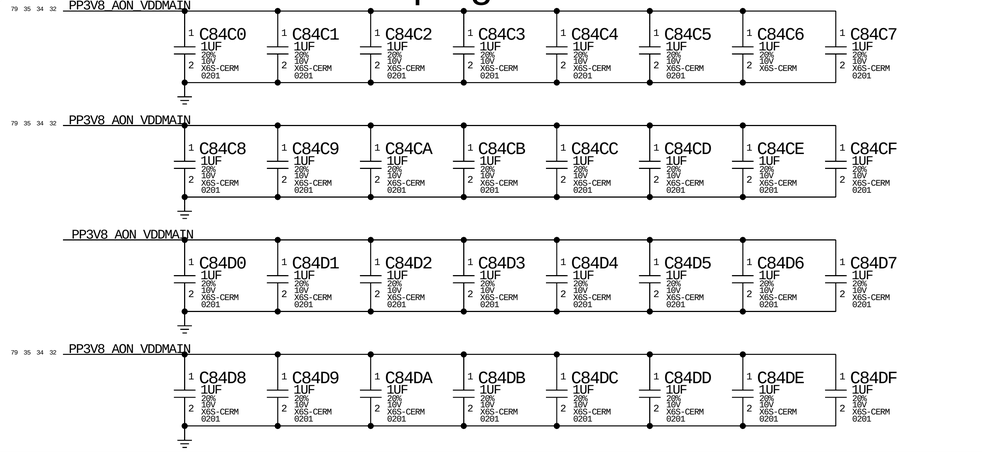
8 | 6 | 5 | 4 | 3

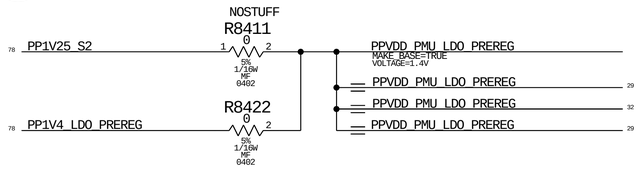
A BUCK 14 Filter



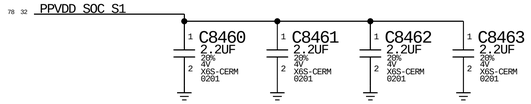
B PMU Main BUCK Decoupling



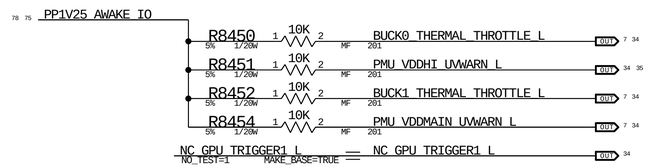
C PPVDD_PMU_LDO_PREREG Aliases



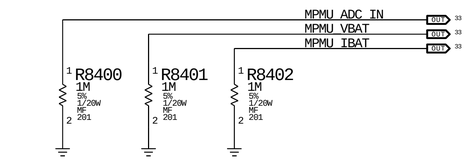
D PPVDD_SOC_S1 Decoupling



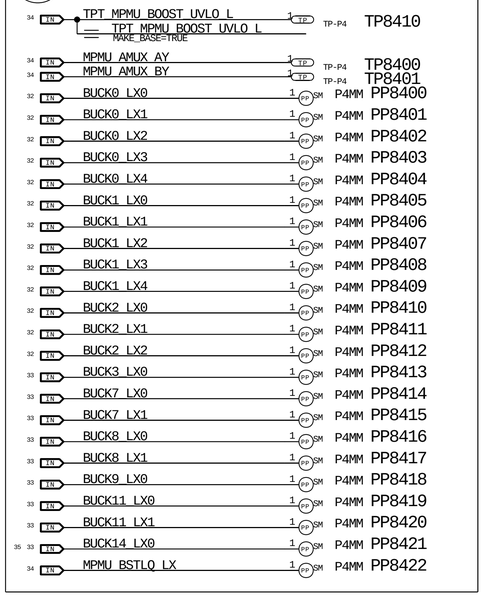
E PMU Control Flag Pull-Ups



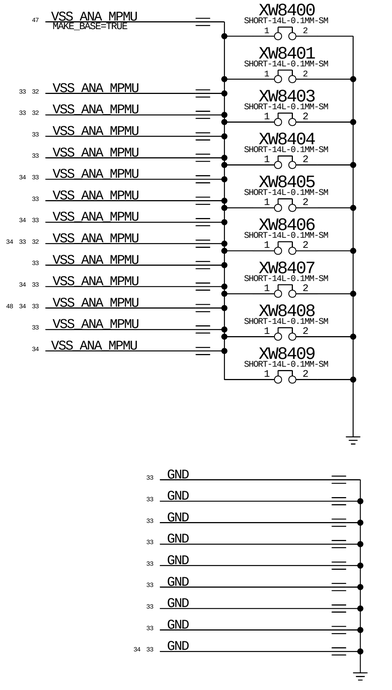
F PMU Input Protection



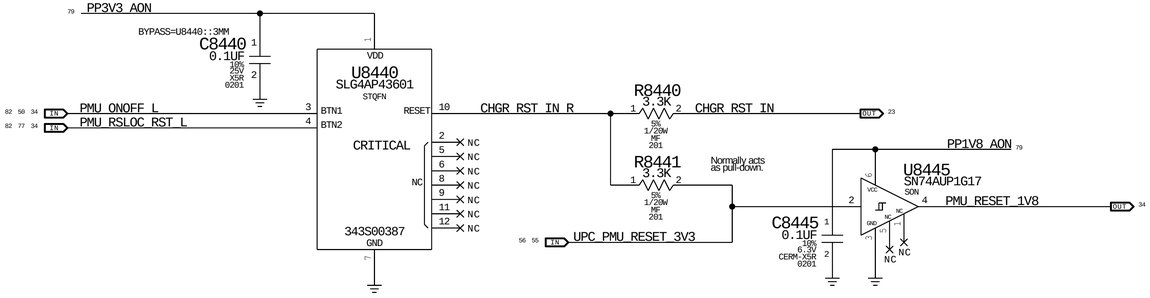
G PMU Test Points



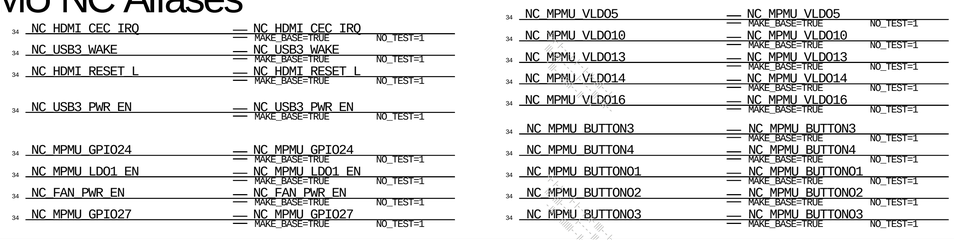
H PMU GND Aliases



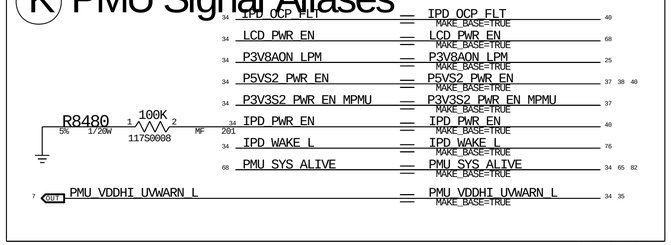
I PMU_RESET_1V8 Generation



J PMU NC Aliases



K PMU Signal Aliases



BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: PMU: Master extra

Apple Inc.

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REVISION: 4.0.0

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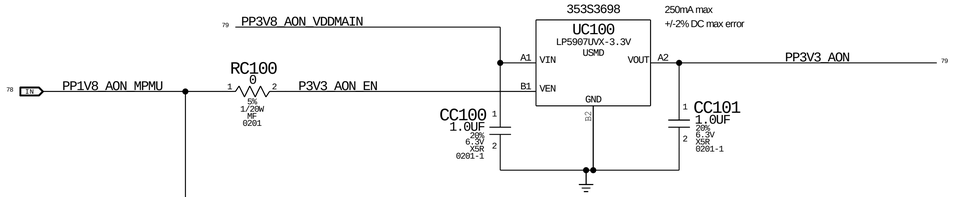
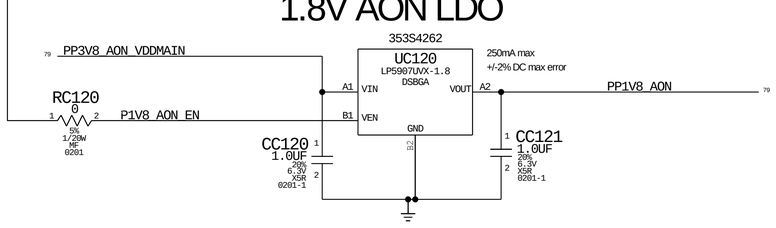
3.3V AON LDO



1.8V AON LDO



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=tga_140 SYNC_DATE=05/31/2019

PAGE TITLE

Power: LDOs

Apple Inc.

DRAWING NUMBER	051-05392
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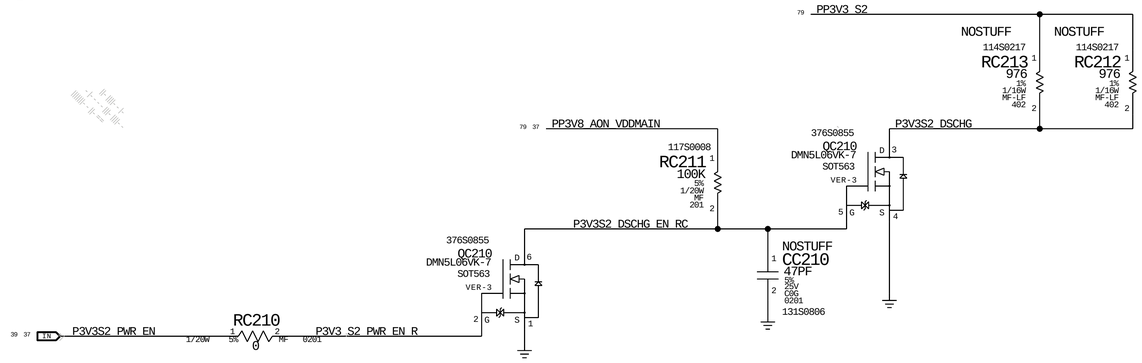
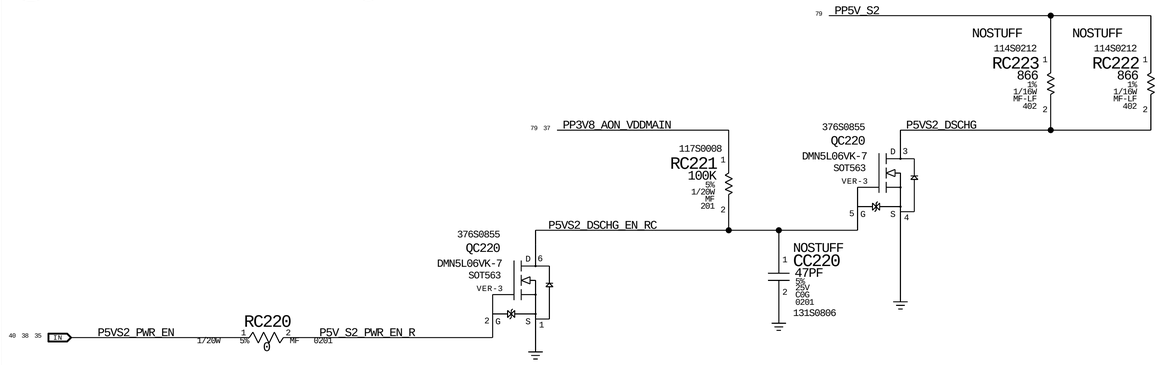
A PP3V3_S2 Discharge Circuit



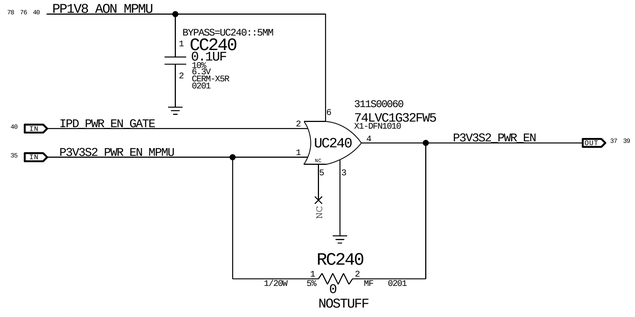
$X1757GHUB/mlb/sim/ltspice/pp3v3_s2_discharge/pp3v3_s2_discharge_diodes_inc.asc

B PP5V_S2 Discharge Circuit



$X1757GHUB/mlb/sim/ltspice/pp5v_s2_discharge/pp5v_s2_discharge_diodes_inc.asc

C P3V3S2_PWR_EN Gating Logic

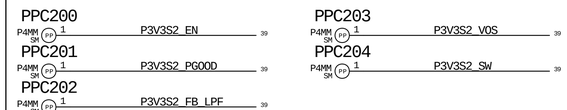


NOTE:
Per Sera PMU OTP, GPIO11 is OFF when the System is OFF.
A side-effect is that during the SIP_SMC->AWAKE transition the rail goes from ON->OFF->ON, which means we lose trackpad power during the OFF transition.

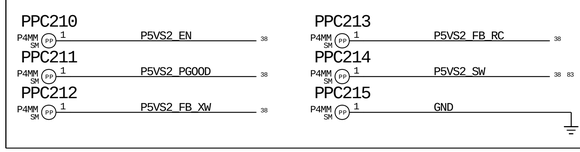
IPD_PWR_EN and PP5V_S2_EN were moved to GPIOs that Sera PMU can "hold" off.

NOSTUFF

D PP3V3_S2 Probe Points



E PP5V_S2 Probe Points



SYNC_MASTER=tga_140 SYNC_DATE=05/31/2019

PAGE TITLE

POWER: 5V, 3V3 Support

Apple Inc.

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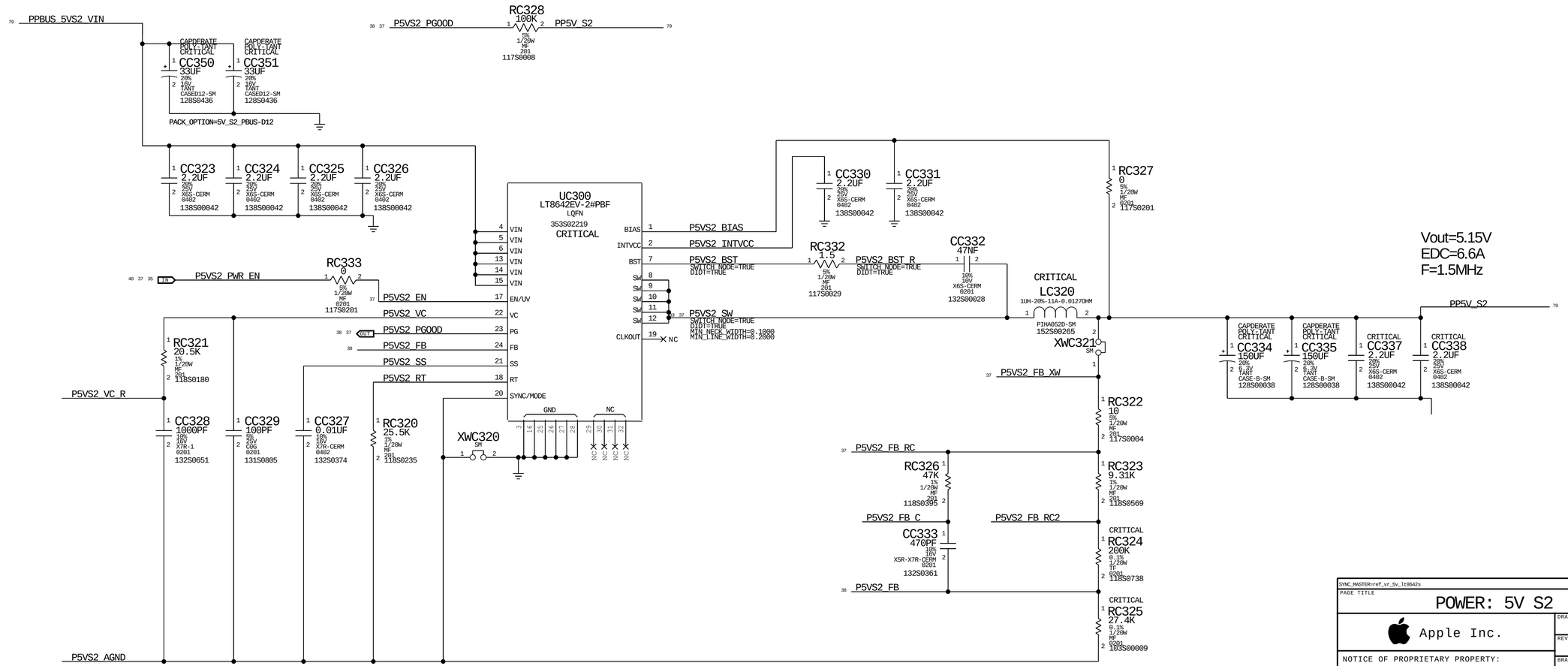
* OK2INTEGRATE *

5V_S2 Voltage Regulator

SET ONE OPTION FOR PBUS CAPS

PACK_OPTION=5V_S2_PBUS-B12
PACK_OPTION=5V_S2_PBUS-D2
PACK_OPTION=5V_S2_PBUS-D12

START UP TIME < 15 MS



SYNC_MASTER=ref_vr_5v_lt8642s SYNC_DATE=05/31/2019

PAGE TITLE

POWER: 5V S2

Apple Inc.

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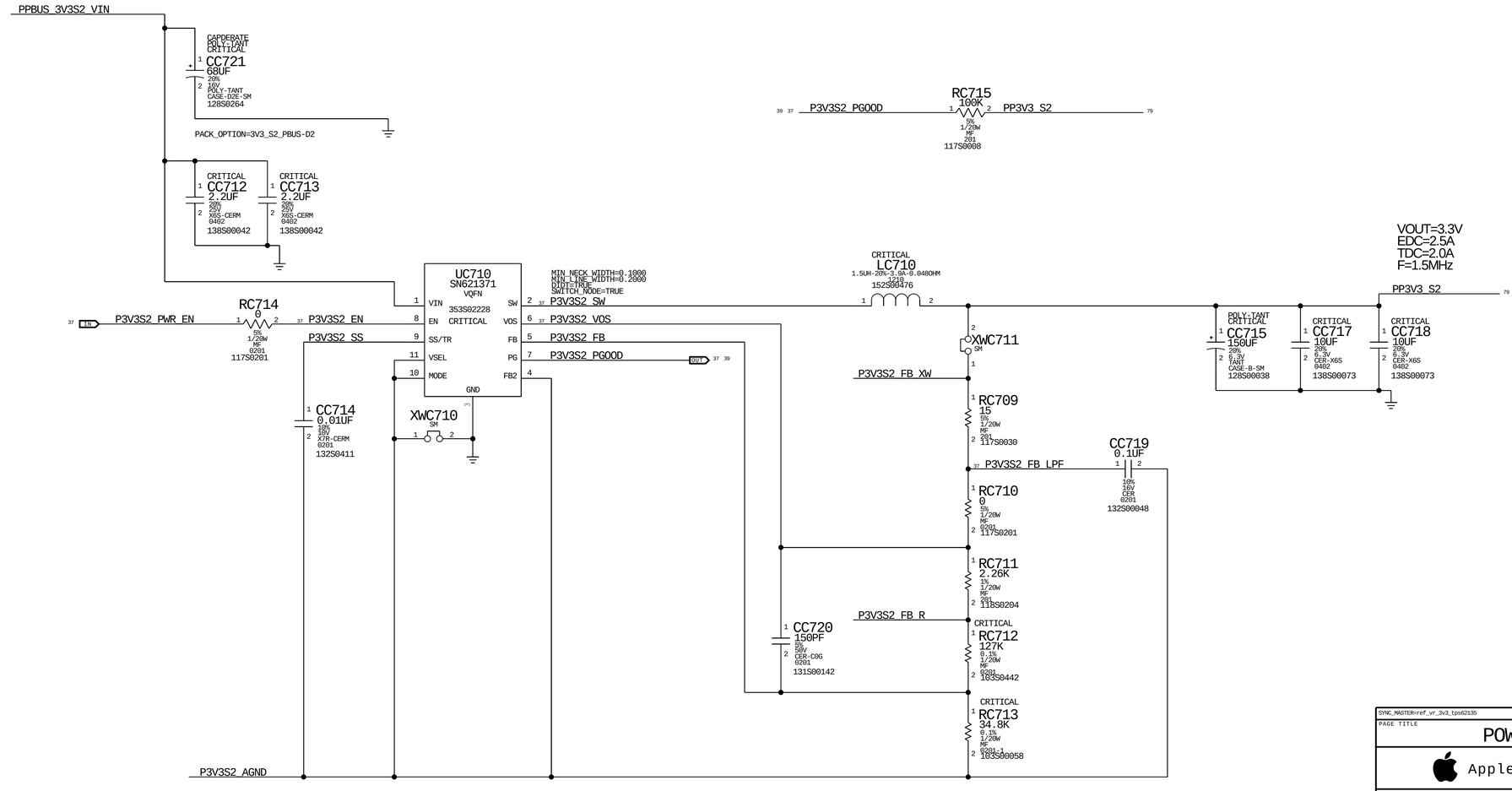
* OK2INTEGRATE *

3V3_S2 VR

SET ONE OPTION FOR PBUS CAPS

PACK_OPTION=3V3_S2_PBUS-B12
PACK_OPTION=3V3_S2_PBUS-D2
PACK_OPTION=3V3_S2_PBUS-D12
PACK_OPTION=3V3_S2_PBUS-25V_D2

START UP TIME <5 MS



SYNC_MASTER=ref_vr_3v3_tps62135 SYNC_DATE=05/31/2019

PAGE TITLE

POWER: 3V3 S2

Apple Inc.

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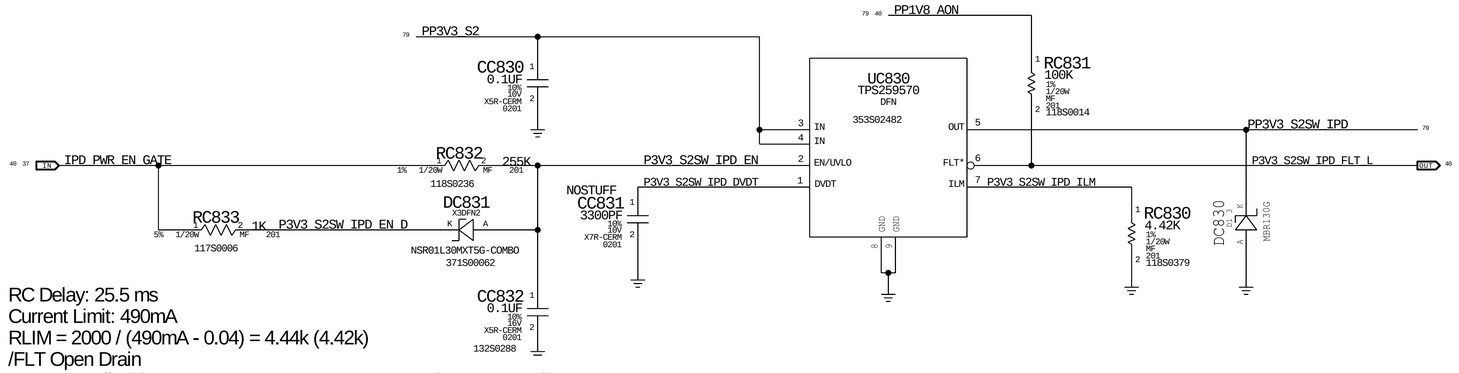
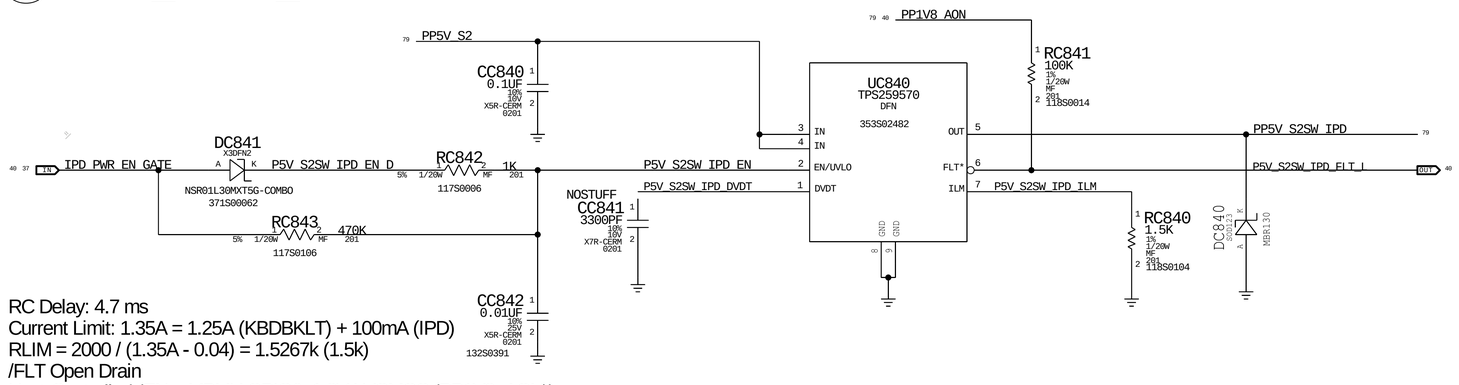
A PP3V3_S2SW_IPD Load Switch & e-Fuse



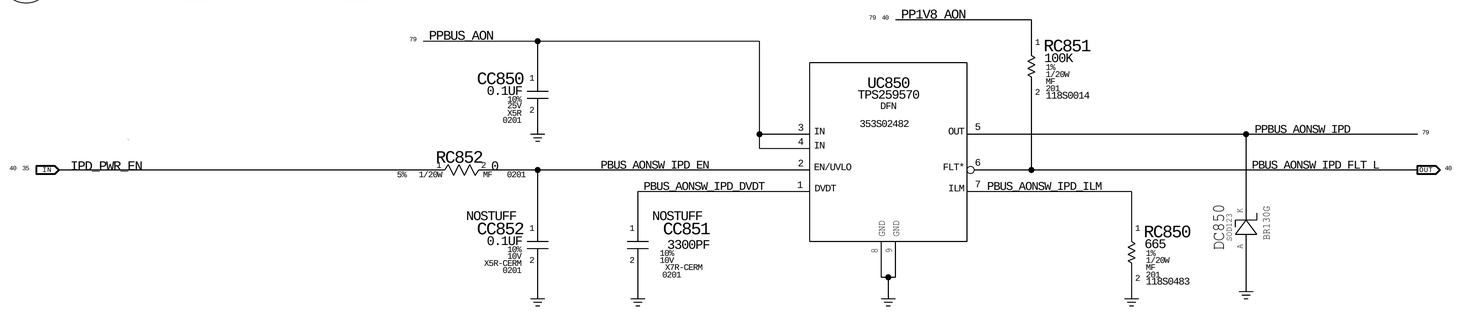
RC Delay: 25.5 ms
Current Limit: 490mA
RLIM = 2000 / (490mA - 0.04) = 4.44k (4.42k)
/FLT Open Drain
Host-Controlled (EN = MPMU GPIO6, 1.8V LVCMOS (PP1V8_AON))
$X1757GHUB/mlb/sim/ltspice/ocp_rc_filters/ocp_filters.asc

B PP5V_S2SW_IPD Load Switch & e-Fuse



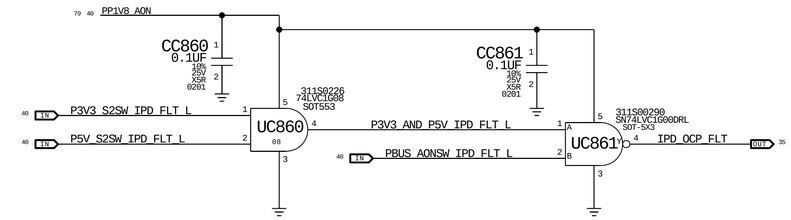
RC Delay: 4.7 ms
Current Limit: 1.35A = 1.25A (KBDBKLT) + 100mA (IPD)
RLIM = 2000 / (1.35A - 0.04) = 1.5267k (1.5k)
/FLT Open Drain
Host-Controlled (EN = MPMU GPIO6, 1.8V LVCMOS (PP1V8_AON))
$X1757GHUB/mlb/sim/ltspice/ocp_rc_filters/ocp_filters.asc

C PPBUS_AONSW_IPD Load Switch & e-Fuse

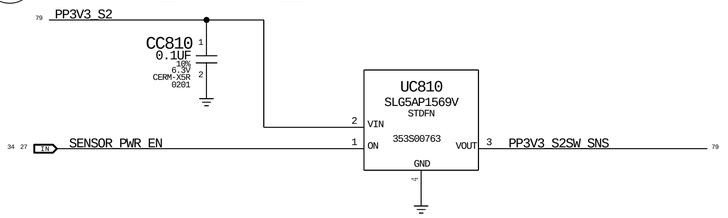


Current Limit: 3A
RLIM = 2000 / (3A - 0.04) = 676 (665)
/FLT Open Drain
Self-Controlled (EN = 3.13V to 5.93V)

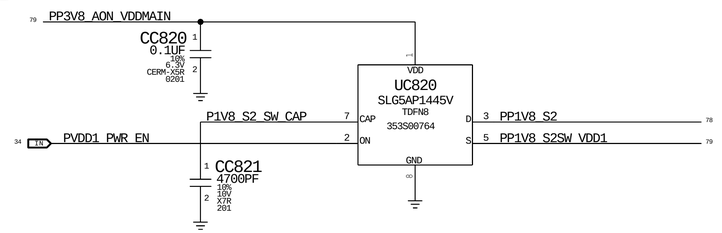
D IPD OCP Fault



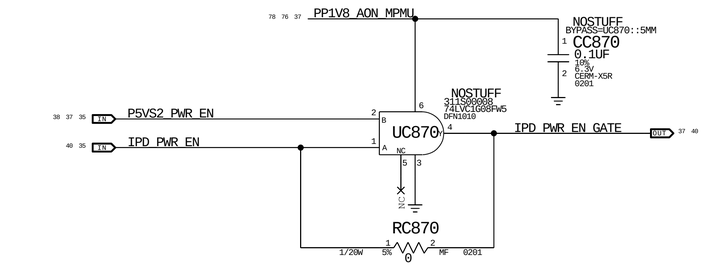
E PP3V3_S2SW_SNS Load Switch



F PP1V8_S2SW_VDD1 Load Switch



G IPD_PWR_EN Gating Logic



SYNC_MASTER=ref_vr_3v3_tps62135 SYNC_DATE=05/31/2019

PAGE TITLE: Power: Load Switches

Apple Inc.

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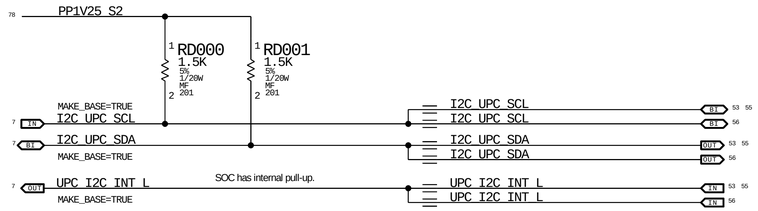
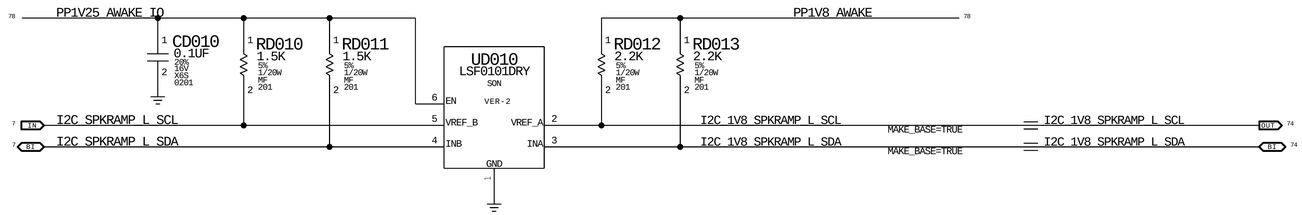
SIO I2C0

DEVICE	DEV	WR	RD
ACE 0	0x38	0x70	0x71
ACE 1	0x3F	0x7E	0x7F



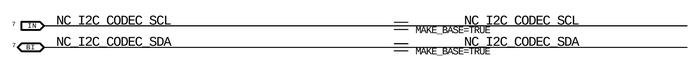
SIO I2C1

DEVICE	DEV	WR	RD
SPKR AMP L	0x31	0x62	0x63



SIO I2C2

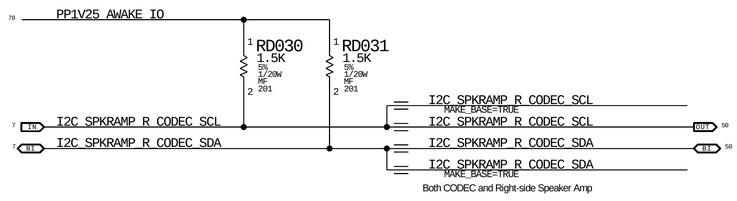
DEVICE	DEV	WR	RD



UNUSED

SIO I2C3

DEVICE	DEV	WR	RD
SPKR AMP R	0x34	0x68	0x69
CODEC	0x48	0x90	0x91



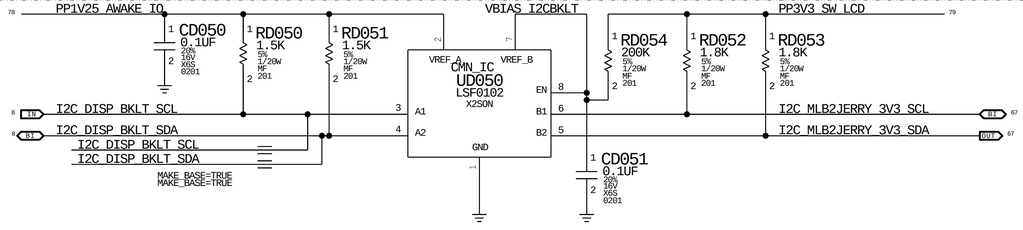
SIO I2C4

DEVICE	DEV	WR	RD

UNUSED

DISP I2C

DEVICE	DEV	WR	RD
LP8549	0x2C	0x58	0x59



BOM_COST_GROUP=SMC

SYNC_MASTER=T668 SYNC_DATE=05/31/2019

PAGE TITLE

I2C: SIO, DISP

Apple Inc.

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ISP I2C0

DEVICE DEV WR RD

UNUSED

ISP I2C1

DEVICE DEV WR RD

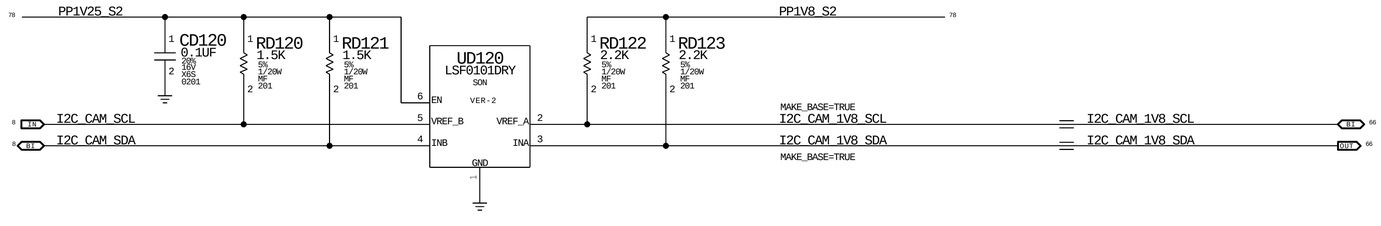
UNUSED

ISP I2C2

DEVICE DEV WR RD

CAMERA 0x10 0x20 0x21

IMAGE SENSOR 0x36 0x6C 0x6D



ISP I2C3

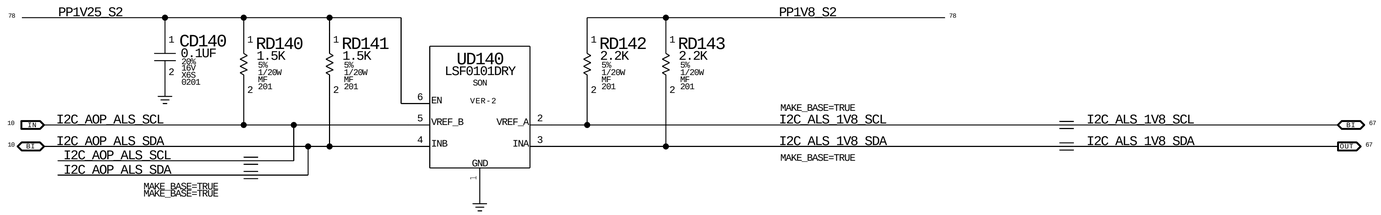
DEVICE DEV WR RD

UNUSED

AOP I2C0

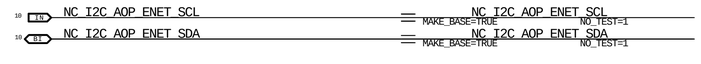
DEVICE DEV WR RD

ALS 0x29 0x52 0x53



AOP I2C1

DEVICE DEV WR RD



UNUSED

SYNC_MASTER=T668 SYNC_DATE=05/31/2019

PAGE TITLE

I2C: ISP, AOP

Apple Inc.

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BRANCH evt-1

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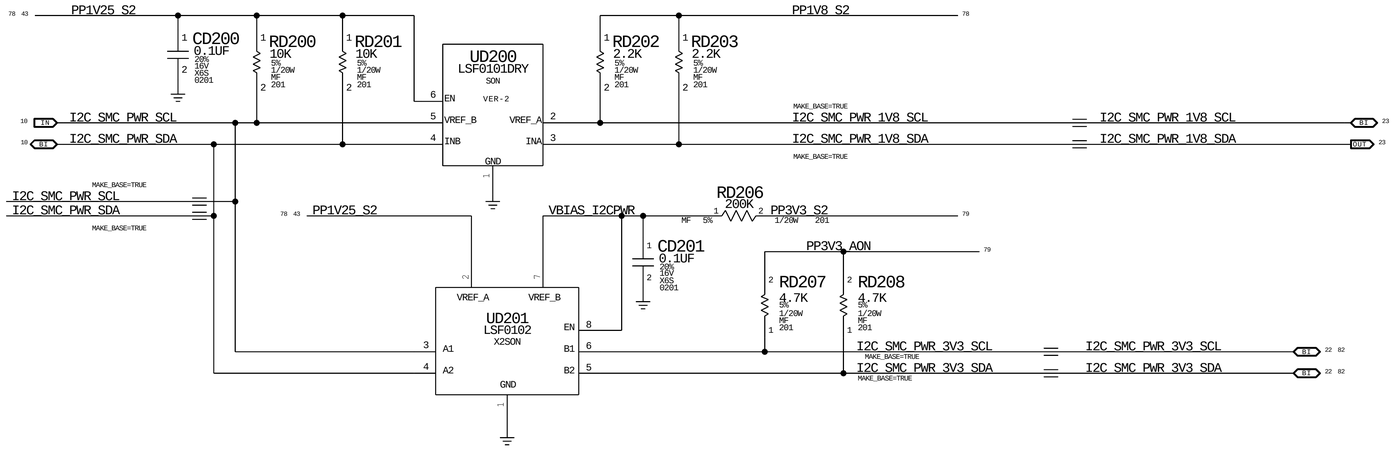
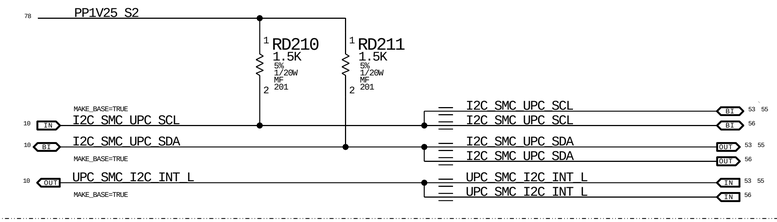
SMC I2C0

DEVICE	DEV	WR	RD
CHARGER	0x09	0x12	0x13
BMU	0x0B	0x16	0x17



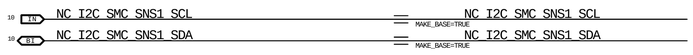
SMC I2C1

DEVICE	DEV	WR	RD
ACE 0	0x38	0x70	0x71
ACE 1	0x3F	0x7E	0x7F



SMC I2C2

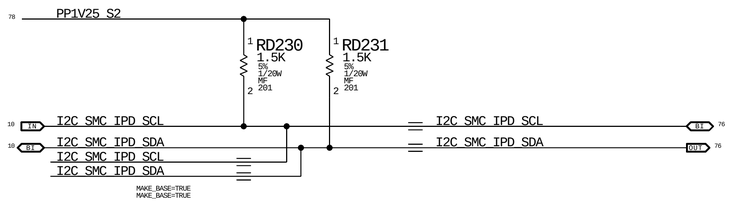
DEVICE	DEV	WR	RD
TBD	0x--	0x--	0x--



UNUSED

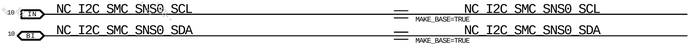
SMC I2C3

DEVICE	DEV	WR	RD
PALM TEMP	0x4C	0x98	0x99



SMC I2C4

DEVICE	DEV	WR	RD
TBD	0x--	0x--	0x--



UNUSED

BOM_COST_GROUP=SMC

SYNC_MASTER=T668 SYNC_DATE=05/31/2019

PAGE TITLE

I2C: SMC

Apple Inc.

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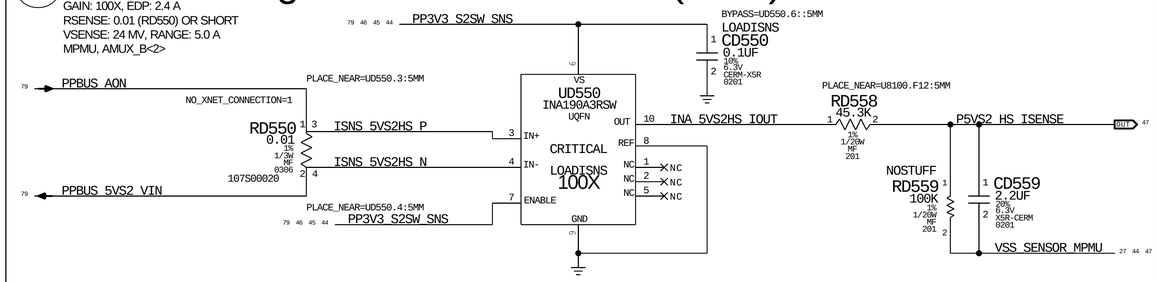
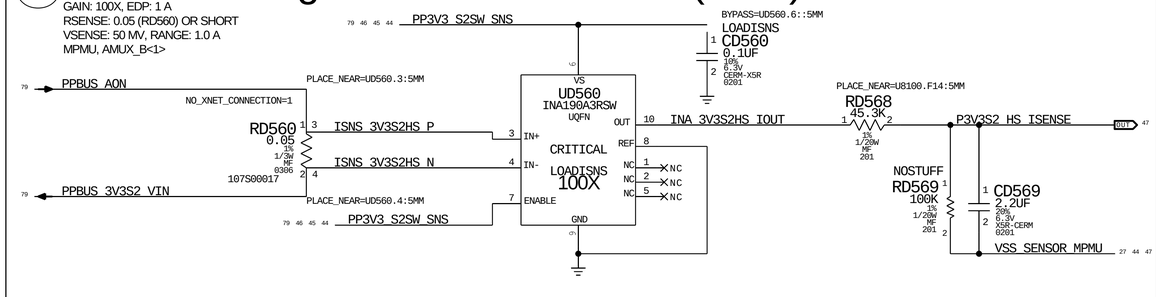
A 5V S2 VR High Side Current Sensor (IO5R)

GAIN: 100X, EDP: 2.4 A
RSENSE: 0.01 (RD550) OR SHORT
VSENSE: 24 MV, RANGE: 5.0 A
MPMU, AMUX_B<2>



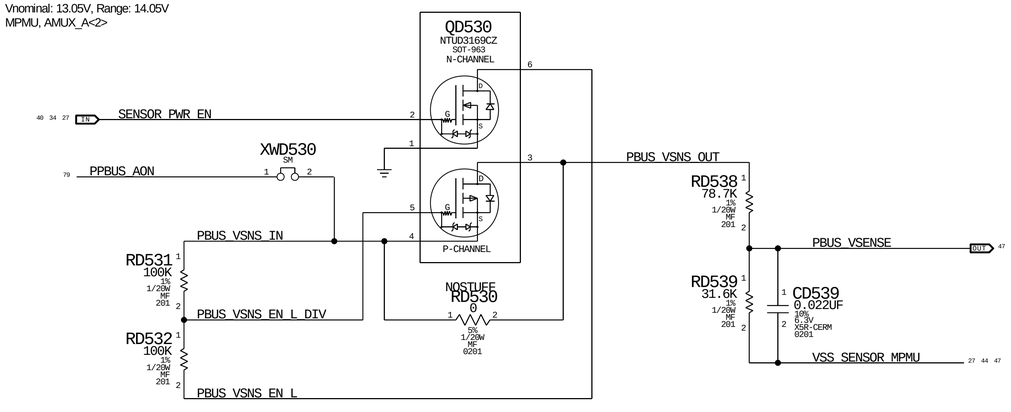
B 3V3 S2 VR High Side Current Sensor (IO3R)

GAIN: 100X, EDP: 1 A
RSENSE: 0.05 (RD560) OR SHORT
VSENSE: 50 MV, RANGE: 1.0 A
MPMU, AMUX_B<1>



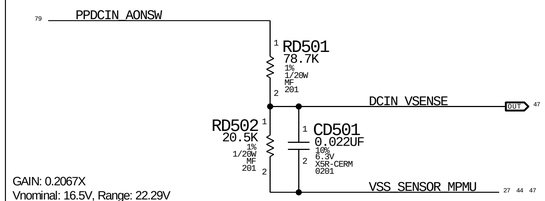
C PPBUS Voltage Sensor (VP0R)

GAIN: 0.2865X
Vnominal: 13.05V, Range: 14.05V
MPMU, AMUX_A<2>



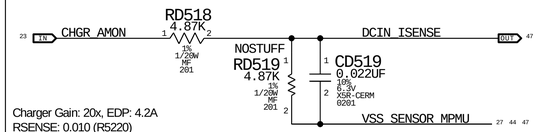
$X1757GHUB/mlb/sim/ltspice/vp0r_sense/vp0r_pbus_vsense_pulse_diodesinc.asc
$X1757GHUB/mlb/sim/ltspice/vp0r_sense/vp0r_pbus_vsense_pulse_onsemi.asc

D DCIN Voltage Sensor (VD0R)



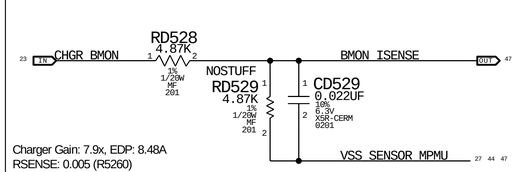
GAIN: 0.2067X
Vnominal: 16.5V, Range: 22.29V
MPMU, AMUX_A<0>

E DCIN Current Sensor (ID0R)



Charger Gain: 20x, EDP: 4.2A
RSENSE: 0.010 (R5220)
MPMU, AMUX_A<1>

F BMON Current Sensor (IPBR)



Charger Gain: 7.9x, EDP: 8.48A
RSENSE: 0.005 (R5260)
MPMU, AMUX_A<3>

SYNC_MASTER=T668 SYNC_DATE=05/31/2019

PAGE TITLE
SENSORS: POWER HIGH SIDE (1/2)

Apple Inc.

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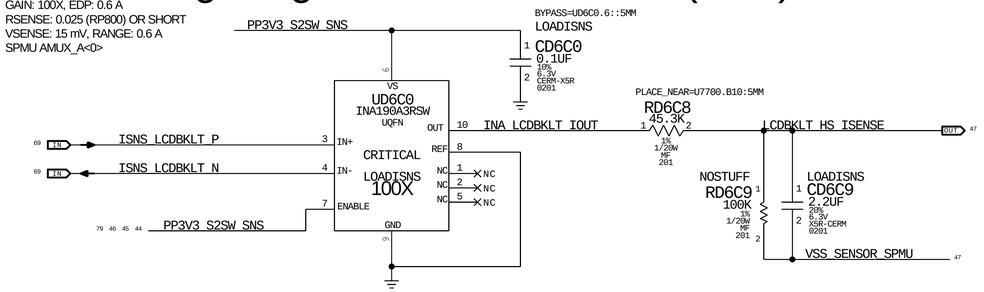
A LCD Backlight High Side Current Sensor (IBLR)

GAIN: 100X, EDP: 0.6 A
RSENSE: 0.025 (RP800) OR SHORT
VSENSE: 15 mV, RANGE: 0.6 A
SPMU AMUX_A<0>



SYNC_MASTER=T668
SYNC_DATE=05/31/2019

PAGE TITLE
SENSORS: POWER HIGH SIDE (2/2)

Apple Inc.

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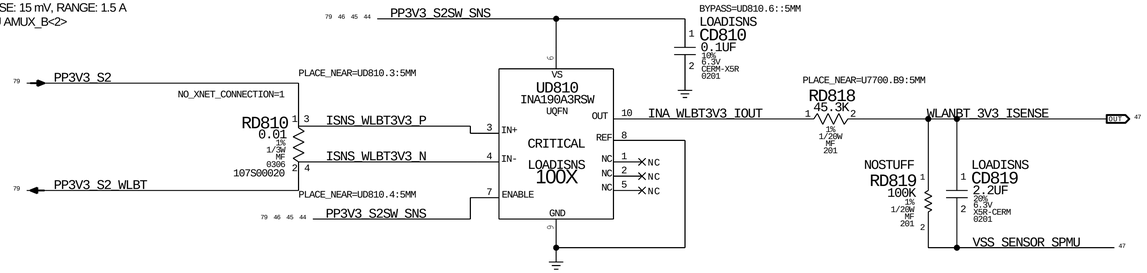
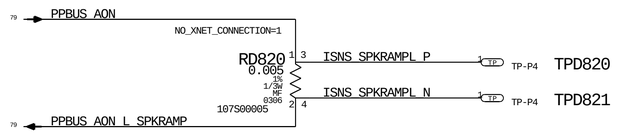
A WLAN BT 3V3 S2 Current Sensor (IW3C)

GAIN: 100X, EDP: 1.5 A
RSENSE: 0.01 (RD810) OR SHORT
VSENSE: 15 mV, RANGE: 1.5 A
SPMU AMUX_B<2>



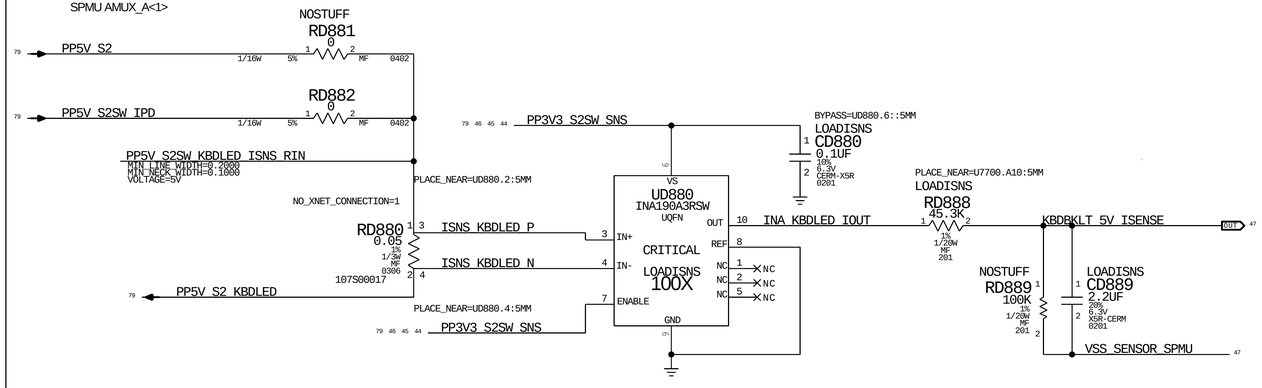
B Left Speaker Amplifier Current Sensor (Ixxx)

GAIN: 100X, EDP: 2.6 A
RSENSE: 0.005 (RD820) OR SHORT
VSENSE: 13 mV, RANGE: 3.3 A



C Keyboard LED 5V Current Sensor (IKBC)

GAIN: 100X, EDP: 0.24 A
RSENSE: 0.05 (RD880) OR SHORT
VSENSE: 12 mV, RANGE: 0.33 A
SPMU AMUX_A<1>



SYNC_MASTER=T668 SYNC_DATE=05/31/2019

PAGE TITLE
SENSORS: POWER LOW SIDE (1/2)

Apple Inc.

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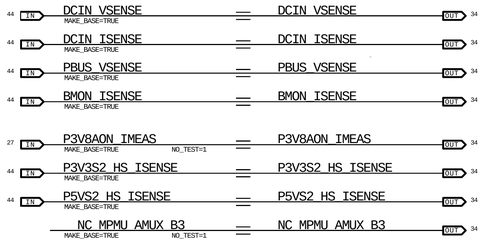
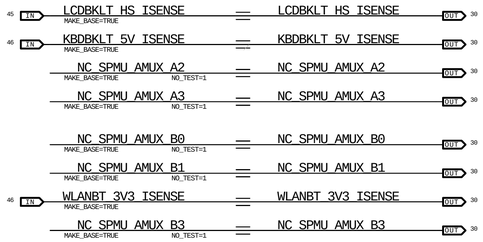
A ADC Input Aliases

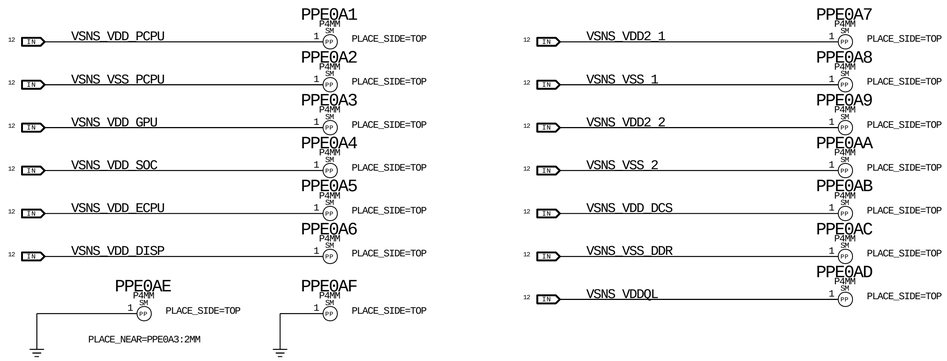
MASTER PMU AMUX ALIAS



SLAVE PMU AMUX ALIAS

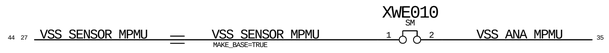


B SOC Sense Lines

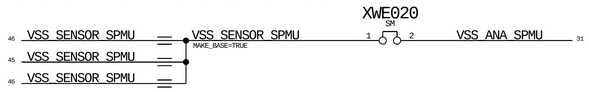


C I/V Sensor Ground Reference Aliases

Master PMU ADC Ground Alias



Slave PMU ADC Ground Alias



SENSORS: POWER SUPPORT

SYNC_MASTER=T668 SYNC_DATE=05/31/2019

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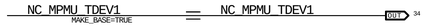
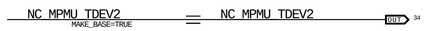
A Master PMU TDEV1 (Txxx)

Location: 3.8V AON VR



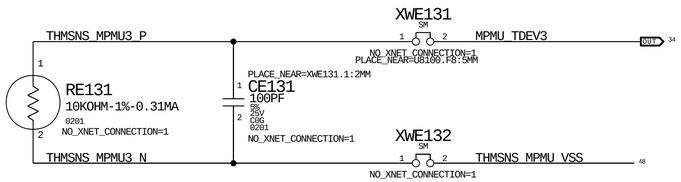
B Master PMU TDEV2 (Txxx)

Location: SoC back side ?



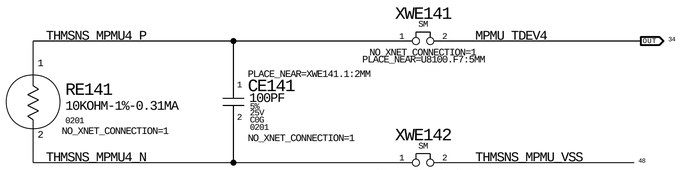
C Master PMU TDEV3 (TIOP)

Location: Thunderbolt Proximity

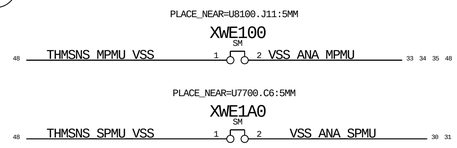


D Master PMU TDEV4 (TWOP)

Location: Wireless Proximity

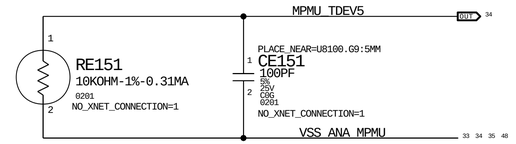


E Master/Slave PMU VSS Connection



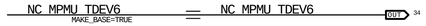
F Master PMU TDEV5 (TPMP)

Location: Master PMU Proximity



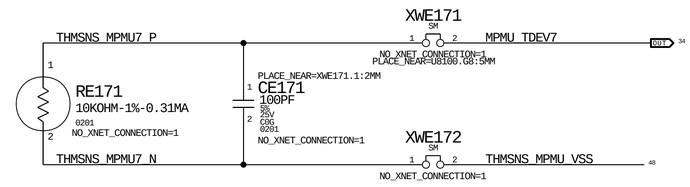
G Master PMU TDEV6 (Txxx)

Location: NAND, TBD



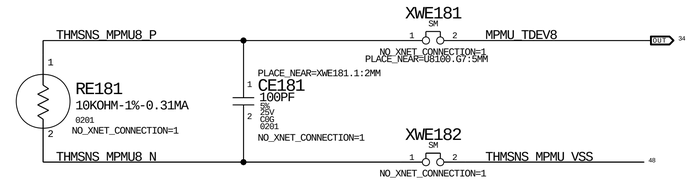
H Master PMU TDEV7 (TCHP)

Location: Charger Proximity



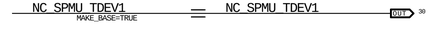
I Master PMU TDEV8 (TMVR)

Location: Main VR (PP3V8_AON_VDDMAIN)



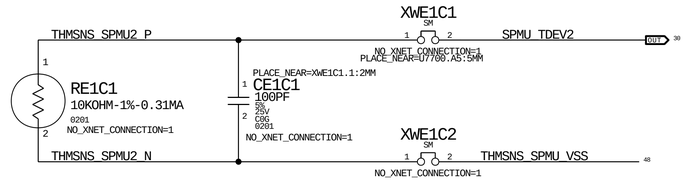
J Slave PMU TDEV1 (Txxx)

Location: TBD



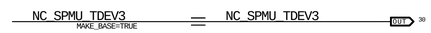
K Slave PMU TDEV2 (TH0T)

Location: NAND Proximity



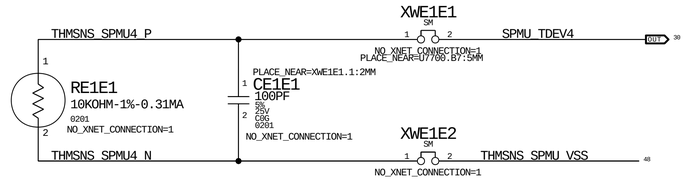
L Slave PMU TDEV3 (Txxx)

Location: TBD



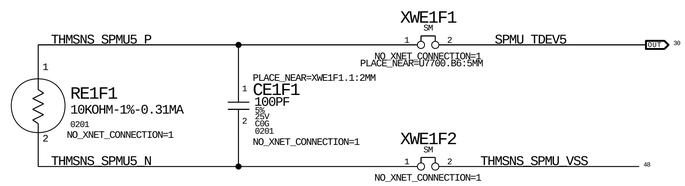
M Slave PMU TDEV4 (TSCD)

Location: SOC Proximity



N Slave PMU TDEV5 (TPSP)

Location: Slave PMU Proximity



SYNC_MASTER=T668 SYNC_DATE=05/31/2019

PAGE TITLE: Sensors: Thermal

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D

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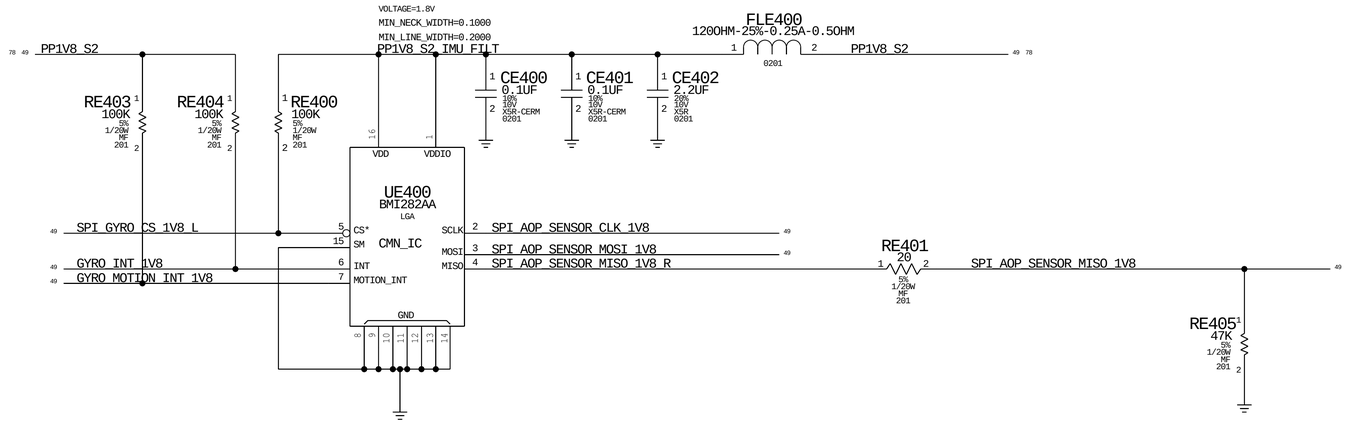
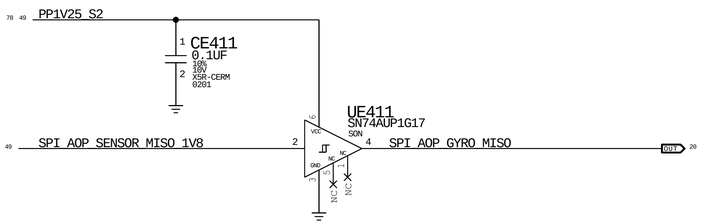
OPEN ITEMS:

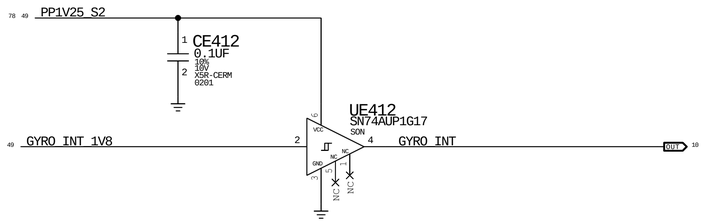
FERRITE IS PLACEHOLDER ONLY
J417 USES 1555S0686 (01005)
MUST FIND PROPER PART, IF ONE IS NEEDED AT ALL

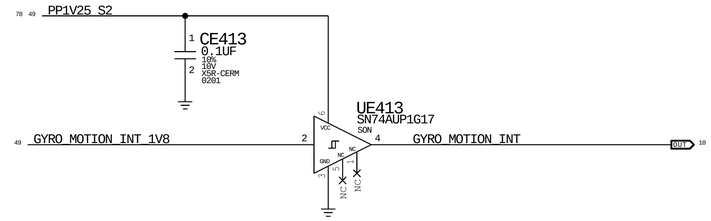
WHAT DOES SM SCAN MODE PIN DO AND WHY IS IT GROUNDED ON J417?

KOBOL: ACCEL & GYRO

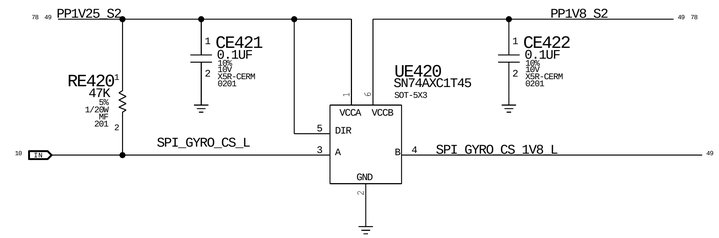


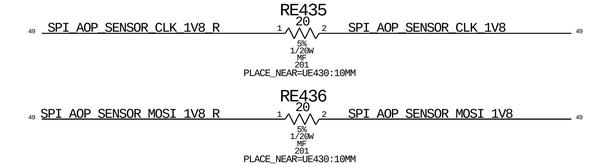


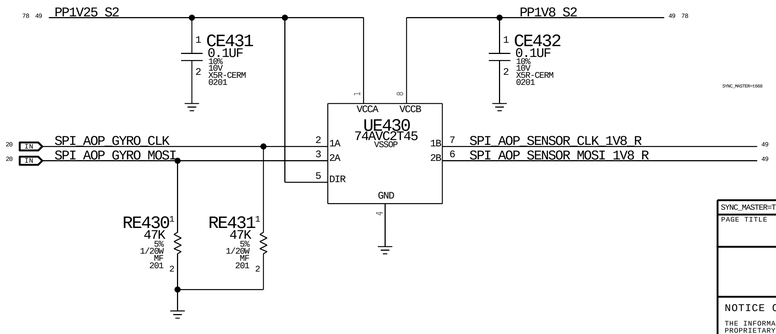




SPI LEVEL TRANSLATION







SYNC_MASTER=T668 SYNC_DATE=05/31/2019

PAGE TITLE
SENSORS: MOTION

Apple Inc.

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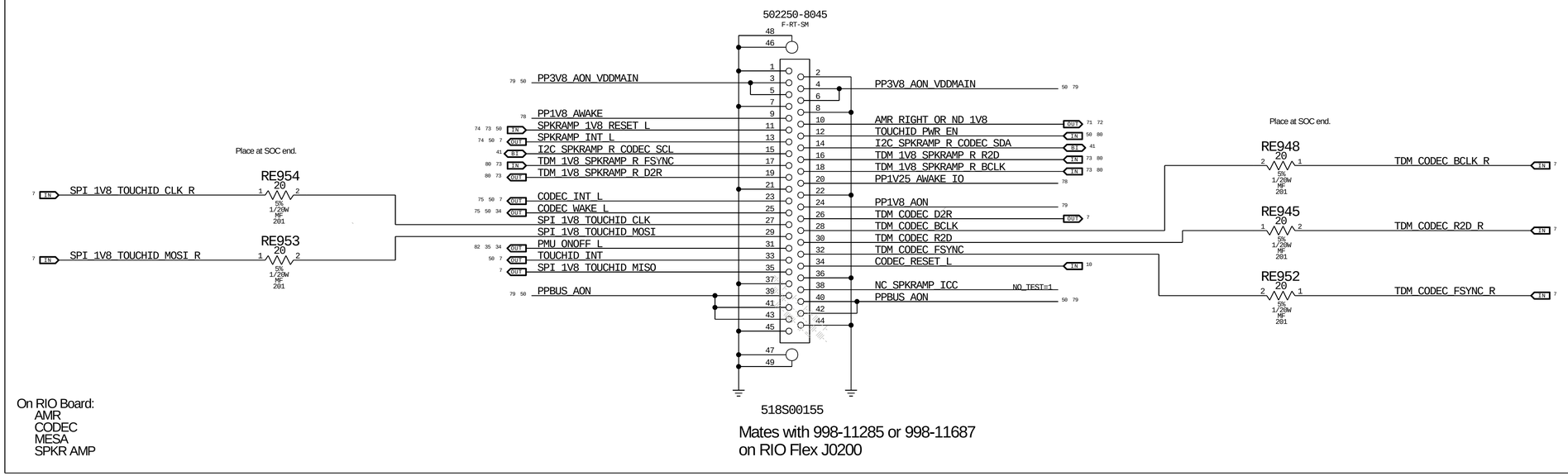
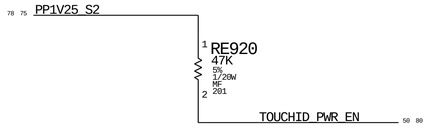
RIO Board Connector



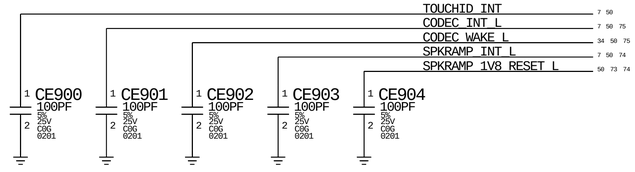
On RIO Board:
- AMR
- CODEC
- MESA
- SPKR AMP

Mates with 998-11285 or 998-11687
on RIO Flex J0200

B TOUCHID Power Enable Pull-Up



C RIO Control Capacitors



SYNC_MASTER=T668 SYNC_DATE=05/31/2019

PAGE TITLE: RIO Connector

Apple Inc.

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** OK2INTEGRATE **

Caps and connector must be aliased to BBR signals.
Lanes 1 and 2 can be swapped, both pairs, both sides; all or nothing.
Inputs can be polarity inverted independently per pair.
All swaps and inversions must be communicated to TBT Firmware team.

USBC HIGH-SPEED AC COUPLING

GND_VOID=TRUE
USBC_ATC0_R2D_C_P<1> — CF020 0.22UF — USBC_ATC0_R2D_P<1>
USBC_ATC0_R2D_C_N<1> — CF021 0.22UF — USBC_ATC0_R2D_N<1>
USBC_ATC0_R2D_C_P<2> — CF024 0.22UF — USBC_ATC0_R2D_P<2>
USBC_ATC0_R2D_C_N<2> — CF025 0.22UF — USBC_ATC0_R2D_N<2>
USBC_ATC0_D2R_P<1> — CF022 0.22UF — USBC_ATC0_D2R_C_P<1>
USBC_ATC0_D2R_N<1> — CF023 0.22UF — USBC_ATC0_D2R_C_N<1>
USBC_ATC0_D2R_P<2> — CF026 0.22UF — USBC_ATC0_D2R_C_P<2>
USBC_ATC0_D2R_N<2> — CF027 0.22UF — USBC_ATC0_D2R_C_N<2>
USBC_ATC0_AUX_P — CF028 0.1UF — USBC_ATC0_AUX_C_P
USBC_ATC0_AUX_N — CF029 0.1UF — USBC_ATC0_AUX_C_N

RF028 33K 5% 1/20W MF 201
RF029 33K 5% 1/20W MF 201

CIO_ATC0_LSTX_3V3 — CIO_ATC0_LSTX_3V3
CIO_ATC0_LSRX_3V3 — CIO_ATC0_LSRX_3V3
NOSTUFF
RF008 100K 5% 1/20W MF 201
RF009 100K 5% 1/20W MF 201

UF000 (338S00561)

9999HH, BGA, SYM 1 OF 2, CRITICAL, OMIT_TABLE

USBC_ATC0_R2D_P<1>	J1	ASSRXP1
USBC_ATC0_R2D_N<1>	J2	ASSRXN1
USBC_ATC0_R2D_P<2>	C1	ASSRXP2
USBC_ATC0_R2D_N<2>	C2	ASSRXN2
USBC_ATC0_D2R_C_P<1>	G1	ASSTXP1
USBC_ATC0_D2R_C_N<1>	G2	ASSTXN1
USBC_ATC0_D2R_C_P<2>	E1	ASSTXP2
USBC_ATC0_D2R_C_N<2>	E2	ASSTXN2
USBC_ATC0_AUX_C_P	L8	PA_AUX_P (INTERNAL CAPS, PU, PD)
USBC_ATC0_AUX_C_N	M8	PA_AUX_N
CIO_ATC0_LSTX_3V3	M7	PA_LSTX_SBU1
CIO_ATC0_LSRX_3V3	L7	PA_LSRX_SBU2
INT_I2C_ATCRTMR0_L	A10	I2C_INT
I2C_UPC0_ATCRTMR0_SCL	C9	I2C_SCL
I2C_UPC0_ATCRTMR0_SDA	E7	I2C_SDA
ATCRTMR0_GPIO_5	B9	POC_GPIO_5
ATCRTMR0_GPIO_6	A8	POC_GPIO_6
ATCRTMR0_FLASH_SHARE_EN	A4	POC_GPIO_10 (PU-69K)
ATCRTMR01_FLASH_MSTR	A5	POC_GPIO_11 (PU-69K)
ATCRTMR0_GPIO_12	A6	POC_GPIO_12 (PU-69K)
ATCRTMR0_THERM_DP	M11	THERMDA
ATCRTMR0_XTAL25M_IN	L9	XTAL_25_IN
ATCRTMR0_XTAL25M_OUT	M9	XTAL_25_OUT
	L12	MONDC_SVR
	A11	MONDC
	M12	TEST_EDM
NC	A12	NC_A12
NC	J6	NC_J6
NC	L3	NC_L3
NC	J5	NC_J5

USBC0_D2R_P<1>	J12	BSSRXP1
USBC0_D2R_N<1>	J11	BSSRXN1
USBC0_D2R_P<2>	C12	BSSRXP2
USBC0_D2R_N<2>	C11	BSSRXN2
USBC0_R2D_CR_P<1>	G12	BSSTXP1
USBC0_R2D_CR_N<1>	G11	BSSTXN1
USBC0_R2D_CR_P<2>	E12	BSSTXP2
USBC0_R2D_CR_N<2>	E11	BSSTXN2
USBC0_AUXLSX_P	M10	BSBU1
USBC0_AUXLSX_N	L10	BSBU2
ATCRTMR01_ACTIVE_READY_3V3	B8	PERST*
ATCRTMR0_RESET_L	L11	RESET*
JTAG_ATCRTMR01_TDI	A3	TDI
JTAG_ATCRTMR0_TMS	C3	TMS
JTAG_ATCRTMR0_TCK	B5	TCK
JTAG_ATCRTMR01_TDO	C5	TDO
SPI_ATCRTMR0_R_MOSI	C6	EE_DI (To SPI Flash)
SPI_ATCRTMR0_R_MISO	B4	EE_DO
SPI_ATCRTMR0_R_CS_L	B6	EE_CS*
SPI_ATCRTMR0_R_CLK	C7	EE_CLK
	B11	TEST_EN
ATCRTMR0_TEST_PWR_GOOD	B3	TEST_PWR_GOOD
ATCRTMR0_RBIAS	L4	RBIAS
ATCRTMR0_RSENSE	L5	RSENSE
	A1	ATEST_P
	A2	ATEST_N
ATCRTMR0_FORCE_PWR	B10	FORCE_PWR
FLASH_BUSY_USBC01_L	A9	FLASH_BUSY*
	B2	FUSE_VQPS_64
NC_SMBUS_ATCRTMR0_SCL	A7	SMBUS_SCL
NC_SMBUS_ATCRTMR0_SDA	B7	SMBUS_SDA

RF006 100 5% 1/20W MF 201
RF007 4.75K 0.5% 1/20W TF 0201
PLACE_NEAR=UF000.L5:2MM
PLACE_NEAR=UF000.L4:2MM

UF000 (338S00561)

9999HH, BGA, SYM 2 OF 2, CRITICAL, OMIT_TABLE

	F6	VCC0P9_SVR_ANA
	G6	
	E9	VCC0P9_SVR_PB_ANA
	G9	
PP0V9_ATCRTMR0_LVR (VOLTAGE=0.9V)	L6	VCC0P9_LVR
	M6	VCC0P9_LVR_SENSE
PP3V3_ATCRTMR0_ANA (VOLTAGE=3.3V)	L2	VCC3P3_ANA
PP0V9_ATCRTMR0_LC (VOLTAGE=0.9V)	J3	VCC0P9_LC
	E5	VCC3P3_LC
	F3	VSS
	F5	
	G5	
	B1	
	B12	VSS_ANA
	D1	
	D11	
	D12	
	D2	
	F1	
	F11	
	F12	
	F2	
	E6	VCC3P3_SX
PP3V3_ATCRTMR0_VCCA (VOLTAGE=3.3V)	J7	VCC3P3A
PP3V3_ATCRTMR0_SVR (VOLTAGE=3.3V)	M4	VCC3P3_SVR
	M5	
PP0V9_ATCRTMR0_SVR_PGND (VOLTAGE=0V)	E3	VCC0P9_SVR
	G3	
PP0V9_ATCRTMR0_SVR_IND (VOLTAGE=0.9V, DIDT=TRUE)	L1	SVR_IND
	M1	
	M2	SVR_VSS
	M3	
	F7	
	F9	
	G7	
	H1	
	H11	
	H12	
	H2	
	J9	VSS_ANA
	K1	
	K11	
	K12	
	K2	

3.3V LDO

PACK_OPTION=PKGS:SMALL_PITCH
ALLOW_APPLE_PREFIX=U

UF015 TLV75533 X2SON-COMBO 353S02112
PP3V8_AON_VDDMAIN — IN
USBC0_3V3LDO_EN_R — EN
OUT — PP3V3_S2SW_USBC0 (PACK_IGNORE=TRUE, PACK_OPTION=PKGS:LARGER_PITCH)
GND, THRM PAD

RF012 100K 5% 1/20W MF 201
CF010 1.0UF 20% 6.3V X5R 0201-1
CF015 1.0UF 20% 6.3V X5R 0201-1

Clock

RF002 0 0201 5% 1/20W MF
ATCRTMR0_XTAL25M_OUT_R — ATCRTMR0_XTAL25M_OUT
CF002 20PF 5% 25V C0G 0201
CF003 20PF 5% 25V C0G 0201
CRITICAL
YF000 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
RF003 0 0201 5% 1/20W MF
ATCRTMR0_XTAL25M_IN_R — ATCRTMR0_XTAL25M_IN

MIN_LINE_WIDTH=0.1400
MIN_NECK_WIDTH=0.0750

PP3V3_S2SW_USBC0
PP3V3_S2SW_USBC0
ATCRTMR0_GPIO_5 — RF050 100K
ATCRTMR0_GPIO_6 — NOSTUFF RF041 100K
ATCRTMR01_ACTIVE_READY_3V3 — RF040 0
ATCRTMR0_FLASH_SHARE_EN — NOSTUFF RF051 100K
ATCRTMR0_GPIO_12 — NOSTUFF RF043 100K
RF045 100K

PP0V9_ATCRTMR0_SVR
CF065 20UF 20% 6.3V X6S-CERM 0402
CF064 20UF 20% 6.3V X6S-CERM 0402
CF063 20UF 20% 6.3V X6S-CERM 0402
CF062 20UF 20% 6.3V X6S-CERM 0402
CF061 4UF 20% 6.3V CER-XSR 0201
CF060 4UF 20% 6.3V CER-XSR 0201
CF050 4UF 20% 6.3V CER-XSR 0201
CF051 4UF 20% 6.3V CER-XSR 0201
CF052 4UF 20% 6.3V CER-XSR 0201
CF053 4UF 20% 6.3V CER-XSR 0201

CF054 10UF 20% 6.3V CERM 0402
CF055 2.2UF 20% 6.3V X5R-CERM 0201
CF056 2.2UF 20% 6.3V X5R-CERM 0201
CF057 2.2UF 20% 6.3V X5R-CERM 0201
CF058 2.2UF 20% 6.3V X5R-CERM 0201

CF043 12PF 5% 25V NP0-C0G 0201
CF030 2.2UF 20% 6.3V X5R-CERM 0201
CF031 10UF 20% 6.3V CERM 0402
CF032 10UF 20% 6.3V CERM 0402
CF033 10UF 20% 6.3V CERM 0402
CF034 10UF 20% 6.3V CERM 0402
CF035 10UF 20% 6.3V CERM 0402
CF038 12PF 5% 25V NP0-C0G 0201
CF039 4UF 20% 6.3V CER-XSR 0201
CF041 4UF 20% 6.3V CER-XSR 0201
CF040 47UF 20% 6.3V CER-XSR 0603

RF000 0 5% 1/16W MF-LF 402
RF001 0 5% 1/16W MF-LF 402
CF036 2.2UF 20% 6.3V X5R-CERM 0201
CF037 2.2UF 20% 6.3V X5R-CERM 0201
CF042 47UF 20% 6.3V CER-X5R 0603
FROM USB-C PORT CONTROLLER (UPC)
PP3V3_S2SW_USBC0

XWF001 SM — NO_XNET_CONNECTION=1
XWF000 SM — PLACE_NEAR=CF032.2:2MM, NO_XNET_CONNECTION=1
PP0V9_ATCRTMR0_SVR

CRITICAL
LF000 0.68UH-20%-4.3A-0.043OHM 0805

XWF030 SM — ATCRTMR0_THERM_DN
PLACE_NEAR=UF000.K11:2MM
NO_XNET_CONNECTION=1
CONNECT TO GND PIN CLOSEST TO THERMDA PIN

BOM_COST_GROUP=TBT

SYNC_MASTER=ref_usbc_ace2 — SYNC_DATE=05/31/2019

PAGE TITLE: USB-C: High Speed ATC0

Apple Inc.

DRAWING NUMBER	051-05392
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REVISION	4.0.0
BRANCH	evt-1
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** OK2INTEGRATE **

Caps and connector must be aliased to BBR signals.
Lanes 1 and 2 can be swapped, both pairs, both sides; all or nothing.
Inputs can be polarity inverted independently per pair.
All swaps and inversions must be communicated to TBT Firmware team.

USBC HIGH-SPEED AC COUPLING

GND_VOID=TRUE
USBC_ATC1_R2D_C_P<1> — CF120 0.22UF — USBC_ATC1_R2D_P<1>
USBC_ATC1_R2D_C_N<1> — CF121 0.22UF — USBC_ATC1_R2D_N<1>
USBC_ATC1_R2D_C_P<2> — CF124 0.22UF — USBC_ATC1_R2D_P<2>
USBC_ATC1_R2D_C_N<2> — CF125 0.22UF — USBC_ATC1_R2D_N<2>
USBC_ATC1_D2R_P<1> — CF122 0.22UF — USBC_ATC1_D2R_C_P<1>
USBC_ATC1_D2R_N<1> — CF123 0.22UF — USBC_ATC1_D2R_C_N<1>
USBC_ATC1_D2R_P<2> — CF126 0.22UF — USBC_ATC1_D2R_C_P<2>
USBC_ATC1_D2R_N<2> — CF127 0.22UF — USBC_ATC1_D2R_C_N<2>
USBC_ATC1_AUX_P — CF128 0.1UF — USBC_ATC1_AUX_C_P
USBC_ATC1_AUX_N — CF129 0.1UF — USBC_ATC1_AUX_C_N

CF120–CF127: 20% 6.3V 0201 X5R
CF128, CF129: 10% 6.3V 0201 CERM-X5R

RF128 33K 5% 1/20W MF 201
RF129 33K 5% 1/20W MF 201

CIO_ATC1_LSTX_3V3 — USBC_ATC1_C_P
CIO_ATC1_LSRX_3V3 — USBC_ATC1_C_N
NOSTUFF
RF108 100K 5% 1/20W MF 201
RF109 100K 5% 1/20W MF 201

UF100
338S00561
9999HH
BGA
SYM 1 OF 2
CRITICAL
OMIT_TABLE

USBC_ATC1_R2D_P<1>	J1	ASSRXP1	BSSRXP1 J12 — USBC1_D2R_P<1>
USBC_ATC1_R2D_N<1>	J2	ASSRXN1	BSSRXN1 J11 — USBC1_D2R_N<1>
USBC_ATC1_R2D_P<2>	C1	ASSRXP2	BSSRXP2 C12 — USBC1_D2R_P<2>
USBC_ATC1_R2D_N<2>	C2	ASSRXN2	BSSRXN2 C11 — USBC1_D2R_N<2>
USBC_ATC1_D2R_C_P<1>	G1	ASSTXP1	BSSTXP1 G12 — USBC1_R2D_CR_P<1>
USBC_ATC1_D2R_C_N<1>	G2	ASSTXN1	BSSTXN1 G11 — USBC1_R2D_CR_N<1>
USBC_ATC1_D2R_C_P<2>	E1	ASSTXP2	BSSTXP2 E12 — USBC1_R2D_CR_P<2>
USBC_ATC1_D2R_C_N<2>	E2	ASSTXN2	BSSTXN2 E11 — USBC1_R2D_CR_N<2>
USBC_ATC1_AUX_C_P	L8	PA_AUX_P	BSBU1 M10 — USBC1_AUXLSX_P
USBC_ATC1_AUX_C_N	M8	PA_AUX_N	BSBU2 L10 — USBC1_AUXLSX_N
	M7	PA_LSTX_SBU1	PERST* B8 — ATCRTMR01_ACTIVE_READY_3V3
	L7	PA_LSRX_SBU2	RESET* L11 — ATCRTMR1_RESET_L
INT_I2C_ATCRTMR1_L	A10	I2C_INT	TDI A3 — JTAG_ATCRTMR01_TDI
I2C_UPC1_ATCRTMR1_SCL	C9	I2C_SCL	TMS C3 — JTAG_ATCRTMR1_TMS
I2C_UPC1_ATCRTMR1_SDA	E7	I2C_SDA	TCK B5 — JTAG_ATCRTMR01_TCK
			TDO C5 — JTAG_ATCRTMR01_TDO
ATCRTMR1_GPIO_5	B9	P0C_GPIO_5	
ATCRTMR1_GPIO_6	A8	P0C_GPIO_6	To SPI Flash: EE_DI C6 — SPI_ATCRTMR1_R_MOSI
ATCRTMR1_FLASH_SHARE_EN	A4	P0C_GPIO_10 (PU-69K)	EE_DO B4 — SPI_ATCRTMR1_R_MISO
ATCRTMR01_FLASH_SLV_L	A5	P0C_GPIO_11 (PU-69K)	EE_CS* B6 — SPI_ATCRTMR1_R_CS_L
ATCRTMR1_GPIO_12	A6	P0C_GPIO_12 (PU-69K)	EE_CLK C7 — SPI_ATCRTMR1_R_CLK
ATCRTMR1_THERM_DP	M11	THERMDA	TEST_EN B11
			TEST_PWR_GOOD B3 — ATCRTMR1_TEST_PWR_GOOD
ATCRTMR1_XTAL25M_IN	L9	XTAL_25_IN	RBIAS L4 — ATCRTMR1_RBIAS
ATCRTMR1_XTAL25M_OUT	M9	XTAL_25_OUT	RSENSE L5 — ATCRTMR1_RSENSE
	L12	MONDC_SVR	ATEST_P A1 — NC
	A11	MONDC	ATEST_N A2 — NC
	M12	TEST_EDM	FORCE_PWR B10 — ATCRTMR1_FORCE_PWR
NC	A12	NC_A12	FLASH_BUSY* A9 — FLASH_BUSY_USBC01_L
NC	J6	NC_J6	FUSE_VQPS_64 B2
NC	L3	NC_L3	
NC	J5	NC_J5	SMBUS_SCL A7 — NC_SMBUS_ATCRTMR1_SCL
			SMBUS_SDA B7 — NC_SMBUS_ATCRTMR1_SDA

RF106 100 5% 1/20W MF 201
RF107 4.75K 0.5% 1/20W TF 0201
PLACE_NEAR=UF100.L5:2MM
PLACE_NEAR=UF100.L4:2MM

PP3V3_S2SW_USBC1
RF150 100K — ATCRTMR1_GPIO_5
NOSTUFF RF141 100K — ATCRTMR1_GPIO_6
ATCRTMR01_ACTIVE_READY_3V3 — RF140 0
NOSTUFF RF151 100K
NOSTUFF RF143 100K — ATCRTMR1_FLASH_SHARE_EN
NOSTUFF RF145 100K — ATCRTMR1_GPIO_12
(all 5% 1/20W MF 201)

ATCRTMR1_XTAL25M_OUT_R — RF102 0 — ATCRTMR1_XTAL25M_OUT
CF102 20PF 5% 25V C0G 0201
CRITICAL YF100 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
CF103 20PF 5% 25V C0G 0201
ATCRTMR1_XTAL25M_IN_R — RF103 0 — ATCRTMR1_XTAL25M_IN

UF100 (SYM 2 OF 2)
338S00561
9999HH
BGA
CRITICAL
OMIT_TABLE

PP0V9_ATCRTMR1_SVR	F6	VCC0P9_SVR_ANA
	G6	
	E9	VCC0P9_SVR_PB_ANA
	G9	
PP0V9_ATCRTMR1_LVR (VOLTAGE=0.9V)	L6	VCC0P9_LVR
	M6	VCC0P9_LVR_SENSE
	E5	VCC3P3_LC
PP3V3_ATCRTMR1_ANA (VOLTAGE=3.3V)	L2	VCC3P3_ANA
PP0V9_ATCRTMR1_LC (VOLTAGE=0.9V)	J3	VCC0P9_LC
	F3	VSS
	F5	
	G5	
	B1	VSS_ANA
	B12	
	D1	
	D11	
	D12	
	D2	
	F1	
	F11	
	F12	
	F2	

CF154 10UF 20% 6.3V CERM 0402
CF155 2.2UF 20% 6.3V X5R-CERM 0201
CF156 2.2UF 20% 6.3V X5R-CERM 0201
CF157 2.2UF 20% 6.3V X5R-CERM 0201
CF158 2.2UF 20% 6.3V X5R-CERM 0201
MIN_LINE_WIDTH=0.1400
MIN_NECK_WIDTH=0.0750

VCC3P3_SX	E6	
VCC3P3A	J7	
VCC3P3_SVR	M4	
	M5	
VCC0P9_SVR	E3	
	G3	
SVR_IND	L1	
	M1	
SVR_VSS	M2	
	M3	
VSS_ANA	F7	
	F9	
	G7	
	H1	
	H11	
	H12	
	H2	
	J9	
	K1	
	K11	
	K12	
	K2	

VOLTAGE=3.3V PP3V3_ATCRTMR1_VCCA
CF143 12PF 5% 25V NP0-C0G 0201
CF130 2.2UF 20% 6.3V X5R-CERM 0201
CF131 10UF 20% 6.3V CERM 0402
RF100 0 5% 1/16W MF-LF 402
RF101 0 5% 1/16W MF-LF 402
CF136 2.2UF 20% 6.3V X5R-CERM 0201
CF137 2.2UF 20% 6.3V X5R-CERM 0201
CF142 47UF 20% 6.3V CER-X5R 0603
FROM USB-C PORT CONTROLLER (UPC)
PP3V3_S2SW_USBC1
XWF101 SM — NO_XNET_CONNECTION=1
PP3V3_ATCRTMR1_SVR
CF132 10UF 20% 6.3V CERM 0402
CF133 10UF 20% 6.3V CERM 0402
CF134 10UF 20% 6.3V CERM 0402
CF135 10UF 20% 6.3V CERM 0402
BYPASS=UF100.M4:M3:3MM
P0V9_ATCRTMR1_SVR_PGND (VOLTAGE=0V)
XWF100 SM — PLACE_NEAR=CF132.2:2MM, NO_XNET_CONNECTION=1
PP0V9_ATCRTMR1_SVR (VOLTAGE=0.9V)
CF138 12PF 5% 25V NP0-C0G 0201
CF139 4UF 20% 6.3V CER-X5R 0201
CF141 4UF 20% 6.3V CER-X5R 0201
CF140 47UF 20% 6.3V CER-X5R 0603
CRITICAL
LF100 0.68UH-20%-4.3A-0.043OHM 0805
PP0V9_ATCRTMR1_SVR_IND (VOLTAGE=0.9V, DIDT=TRUE)
XWF130 SM — ATCRTMR1_THERM_DN
PLACE_NEAR=UF100.K11:2MM
NO_XNET_CONNECTION=1
CONNECT TO GND PIN CLOSEST TO THERMDA PIN

3.3V LDO

PACK_OPTION=PKGS:SMALL_PITCH
ALLOW_APPLE_PREFIX=U
UF115 TLV75533 X2SON-COMBO 353S02112
PP3V8_AON_VDDMAIN — IN
USBC1_3V3LDO_EN_R — EN
OUT — PP3V3_S2SW_USBC1
GND, THRM PAD
RF112 100K 5% 1/20W MF 201
CF110 1.0UF 20% 6.3V X5R 0201-1
CF115 1.0UF 20% 6.3V X5R 0201-1
PACK_IGNORE=TRUE
PACK_OPTION=PKGS:LARGER_PITCH

BOM_COST_GROUP=TBT

SYNC_MASTER=ref_usbc_ace2 — SYNC_DATE=05/31/2019
PAGE TITLE: USB-C: High Speed ATC1

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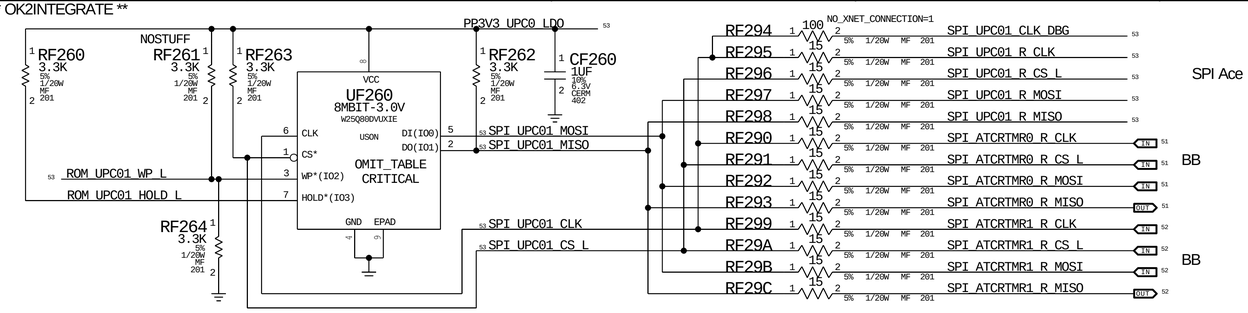
** OK2INTEGRATE **



Ace 0 is SPI Ace?

PACK_OPTION=USBC_SPI_UPC0

SPI_UPC01_R_CLK — MAKE_BASE=TRUE — SPI_UPC01_R_CLK (IN)
SPI_UPC01_R_CS_L — MAKE_BASE=TRUE — SPI_UPC01_R_CS_L (IN)
SPI_UPC01_R_MOSI — MAKE_BASE=TRUE — SPI_UPC01_R_MOSI (IN)
SPI_UPC01_R_MISO — MAKE_BASE=TRUE — SPI_UPC01_R_MISO (OUT)
ROM_UPC01_WP_L — MAKE_BASE=TRUE — ROM_UPC01_WP_L (IN)
SWD_UPC_SWCLK — MAKE_BASE=TRUE — SWD_UPC_SWCLK (IN)
SWD_UPC_SWDIO0 — MAKE_BASE=TRUE — SWD_UPC_SWDIO0 (BI)
PP3V3_UPC0_LDO — MAKE_BASE=TRUE — PP3V3_UPC0_LDO (OUT)

(Internal pull-up) Master should be on SPI Ace2.

PP3V3_S2SW_USBC0 — NOSTUFF — RF244 100K 5% 1/20W MF 201 — ATCRTMR01_FLASH_MSTR (OUT)

FLASH_BUSY_USBC01_L — MAKE_BASE=TRUE — FLASH_BUSY_USBC01_L (BI)

Ace 1 is UART Ace?

PACK_OPTION=USBC_SPI_UPC0

GND (IN)
GND (IN) — MAKE_BASE=TRUE
GND (IN)
GND (OUT)

SWD_UPC01_UART_CLK — MAKE_BASE=TRUE — SWD_UPC01_UART_CLK (IN)
SWD_UPC01_UART_DATA — MAKE_BASE=TRUE — SWD_UPC01_UART_DATA (BI)

RF247 2.2K 5% 1/20W MF 201 — ATCRTMR01_FLASH_SLV_L (OUT)
RF272 100K 5% 1/20W MF 201 — PD_UPC1_GPIO1 (BI)
RF273 100K 5% 1/20W MF 201 — PD_UPC1_HPD (OUT)

SPI Ace: UART_UPC01_TX (IN) — UART_UPC01_TX — MAKE_BASE=TRUE — UART_UPC01_TX (OUT) UART Ace
SPI Ace: UART_UPC01_RX (OUT) — UART_UPC01_RX — MAKE_BASE=TRUE — UART_UPC01_RX (IN) UART Ace

ACE ARKANOID CONN

JF200 — USBC_DBG — 505070-1222 M-ST-SM

SMC		SOC
ATCRTMR0_RESET_L	1 2	UPC_I2C_INT_L
I2C_SMC_UPC_SCL	3 4	I2C_UPC_SDA
I2C_SMC_UPC_SDA	5 6	I2C_UPC_SCL
UPC_SMC_I2C_INT_L	7 8	UPC0_SER_DBG
SPI_UPC01_CLK_DBG	9 10	UPC1_SER_DBG
UART_UPC01_TX	11 12	UART_UPC01_RX
SPI Ace	13 14	SPI Ace
	15 16	

BRIDGE ARKANOID CONN

JF201 — USBC_DBG — 505070-1222 M-ST-SM

ATCRTMR0_FORCE_PWR	1 2	INT_I2C_UPC0_ATCRTMR0_L
PP3V3_S2SW_USBC0	3 4	I2C_UPC0_ATCRTMR0_SCL
PP0V9_ATCRTMR0_LC	5 6	I2C_UPC0_ATCRTMR0_SDA
ATCRTMR01_ACTIVE_READY_3V3	7 8	ATCRTMR1_FORCE_PWR
PP3V3_S2SW_USBC1	9 10	INT_I2C_UPC1_ATCRTMR1_L
I2C_UPC1_ATCRTMR1_SDA	11 12	I2C_UPC1_ATCRTMR1_SCL
	13 14	
	15 16	

USBC_DBG

RF280 200K 1% 1/20W MF 201 — VREFB_ARDV01 — PP3V3_S2_UPC

PP1V25_S2 — CF281 0.1UF 10% 6.3V CERM-X5R 0201 — PACK_OPTION=PKGS:SMALL_PITCH — CF280 0.1UF 10% 6.3V CERM-X5R 0201

UF280 LSF0102 X2SON 311S00234 (VREF_A, VREF_B, EN, A1, A2, B1, B2, GND)

I2C_UPC_SCL — I2C_UPC01_3V3_SCL
I2C_UPC_SDA — I2C_UPC01_3V3_SDA

RF282 5.1K 5% 1/20W MF 201
RF283 5.1K 5% 1/20W MF 201

AARDVARKANOID CONN

JF202 — USBC_DBG — 505070-1222 M-ST-SM

SPI ACE

PP1V25_S2	1 2	SPI_UPC01_CS_L
SWD_UPC_SWDIO0	3 4	SPI_UPC01_CLK
SWD_UPC_SWCLK	5 6	SPI_UPC01_MOSI
SPI_UPC01_MISO	7 8	SWD_UPC01_UART_CLK
I2C_UPC01_3V3_SDA	9 10	SWD_UPC01_UART_DATA
I2C_UPC01_3V3_SCL	11 12	PP1V25_S2
	13 14	
	15 16	

UART ACE

BOM_COST_GROUP=USB-C

ATC0: I2C_ADDR=GND, I2CM_*_CNFG=1Mu03a9 3V3_LDO_X pull-ups
ATC1: I2C_ADDR=Float, I2CM_*_CNFG=1Mu03a9 3V3_LDO_X pull-ups
ATC2: I2C_ADDR=GND, I2CM_*_CNFG=1Mu03a9 pull-downs
ATC3: I2C_ADDR=Float, I2CM_*_CNFG=1Mu03a9 pull-downs

GND — MAKE_BASE=TRUE
NC_UPC1_I2C_ADDR — MAKE_BASE=TRUE — NC_UPC1_I2C_ADDR NO_TEST=1

Configure to enable VDDIO and use it for SWD.

GND
GND — MAKE_BASE=TRUE

PP3V3_UPC0_LDO — RF242 10K 5% 1/20W MF 201 — FLASH_BUSY_USBC01_L MAKE_BASE=TRUE (OUT)

INT_I2C_ATCRTMR0_L — RF210 0 5% 1/20W MF 0201 — UPC_ATCRTMR_INT
INT_I2C_EUSBLS0_L — RF211 0 5% 1/20W MF 0201 — UPC_EUSBLS_INT — INT_I2C_UPC0_ATCRTMR0_L (OUT)
INT_I2C_ATCRTMR1_L — RF215 0 5% 1/20W MF 0201 — UPC_ATCRTMR_INT
INT_I2C_EUSBLS1_L — RF216 0 5% 1/20W MF 0201 — UPC_EUSBLS_INT — INT_I2C_UPC1_ATCRTMR1_L (OUT)

Is UPCx_5V_EN being used?

UPC0_5V_EN — RF234 100K 5% 1/20W MF 201
UPC1_5V_EN — RF235 100K 5% 1/20W MF 201

PACK_OPTION=USBC01_VR5V_LOCAL_NO

PP3V3_S2_UPC

RF220 10K	JTAG_ATCRTMR01_TCK	JTAG_ATCRTMR01_TCK (OUT)
RF221 10K	JTAG_ATCRTMR0_TMS	JTAG_ATCRTMR0_TMS (OUT)
RF222 100K	JTAG_ATCRTMR1_TMS	JTAG_ATCRTMR01_TDI (OUT)
RF223 100K	JTAG_ATCRTMR01_TDI	JTAG_ATCRTMR01_TDO (IN)
RF224 10K	JTAG_ATCRTMR01_TDO	JTAG_ATCRTMR01_TCK (OUT)
		JTAG_ATCRTMR1_TMS (OUT)
		JTAG_ATCRTMR01_TDI (OUT)
		JTAG_ATCRTMR01_TDO (IN)

PP1V25_S2 — CF230 0.1UF 10% 6.3V CERM-X5R 0201 — UF230 311S00243 SN74AXC1T45 SOT-5X3 (VCCA, VCCB, DIR, A, B, GND) — CF231 0.1UF 10% 6.3V CERM-X5R 0201 — PP3V3_S2_UPC

PMU_ACTIVE_READY — ATCRTMR01_ACTIVE_READY_3V3

HV POWER ALIASES

Fuses for laptop charging.

PACK_OPTION=USBC_LAPTOP

CRITICAL 0603-1 FF200 6A-32V — PPDCIN_AONSW — PLACE_NEAR=UF400:5MM — PPHV_INT0_AONSW MAKE_BASE=TRUE VOLTAGE=20V — PPHV_INT0_AONSW
CRITICAL 0603-1 FF201 6A-32V — PPHV_INT1_AONSW — PLACE_NEAR=UF500:5MM — PPHV_INT1_AONSW MAKE_BASE=TRUE VOLTAGE=20V — PPHV_INT1_AONSW

PPVBUS_USBC0 — MAKE_BASE=TRUE — PPVBUS_USBC0
PPVBUS_USBC1 — MAKE_BASE=TRUE — PPVBUS_USBC1

SYNC_MASTER=rvf_usbc_ace2 SYNC_DATE=05/31/2019

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** OK2INTEGRATE **

Ace 0 is Debug Port?

PACK_OPTION=USBC_DEBUG_UPC0

ATC0 / UPC0 / RTMR0

7	IN	UART_DEBUGPRT_R2D	MAKE_BASE=TRUE	=	UART_DEBUGPRT_R2D	IN 54 55
7	OUT	UART_DEBUGPRT_D2R	MAKE_BASE=TRUE	=	UART_DEBUGPRT_D2R	IN 54 55
10	BI	SWD_SOC_SWCLK	MAKE_BASE=TRUE	=	SWD_SOC_SWCLK	OUT 54 55
10	BI	SWD_SOC_SWDIO	MAKE_BASE=TRUE	=	SWD_SOC_SWDIO	OUT 54 55
10	IN	UART_SMC_DEBUGPRT_R2D	MAKE_BASE=TRUE	=	UART_SMC_DEBUGPRT_R2D	OUT 54 55
10	OUT	UART_SMC_DEBUGPRT_D2R	MAKE_BASE=TRUE	=	UART_SMC_DEBUGPRT_D2R	IN 54 55
80	BI	USB_DBG_LS_P	MAKE_BASE=TRUE	=	USB_DBG_LS_P	BI 54 55
80	BI	USB_DBG_LS_N	MAKE_BASE=TRUE	=	USB_DBG_LS_N	BI 54 55
		PP1V8_S2		=	PP1V8_S2	BI 54 55 58
		PP1V8_S2		=	PP1V8_S2	BI 54 58
80	OUT	SOC_DOCK_CONNECT		=	SOC_DOCK_CONNECT	IN 54 55
82 20 6	IN	SOC_DFU_STATUS	MAKE_BASE=TRUE	=	SOC_DFU_STATUS	OUT 54 55
82 34 6	OUT	SOC_FORCE_DFU	MAKE_BASE=TRUE	=	SOC_FORCE_DFU	IN 54 55

Ace 1 is non-debug Port?

ATC1 / UPC1 / RTMR1

PACK_OPTION=USBC_DEBUG_UPC0

	PP1V8_S2		=	PP1V8_S2	BI 54 56 58
	PP1V8_S2		=	PP1V8_S2	BI 54 58
RF320 1/20W	1 5% 2 MF 100K 201	PD_UPC1_DBG0_R	MAKE_BASE=TRUE =	PD_UPC1_DBG0_R	BI 54 56
RF321 1/20W	1 5% 2 MF 100K 201	PD_UPC1_DBG1_R	MAKE_BASE=TRUE =	PD_UPC1_DBG1_R	BI 54 56
RF322 1/20W	1 5% 2 MF 100K 201	PD_UPC1_DBG2_R	MAKE_BASE=TRUE =	PD_UPC1_DBG2_R	BI 54 56
RF323 1/20W	1 5% 2 MF 100K 201	PD_UPC1_DBG3_R	MAKE_BASE=TRUE =	PD_UPC1_DBG3_R	BI 54 56
RF324 1/20W	1 5% 2 MF 100K 201	PD_UPC1_DBG4_R	MAKE_BASE=TRUE =	PD_UPC1_DBG4_R	BI 54 56
RF325 1/20W	1 5% 2 MF 100K 201	PD_UPC1_DBG5_R	MAKE_BASE=TRUE =	PD_UPC1_DBG5_R	BI 54 56
RF328 1/20W	1 5% 2 MF 100K 201	PD_UPC1_USBP2_RP	MAKE_BASE=TRUE =	PD_UPC1_USBP2_RP	BI 54 56
RF329 1/20W	1 5% 2 MF 100K 201	PD_UPC1_USBP2_RN	MAKE_BASE=TRUE =	PD_UPC1_USBP2_RN	BI 54 56

Ace2 GPIOs

RF373 1/20W	1 5% 2 MF 100K 201	PD_UPC1_GPIO7	MAKE_BASE=TRUE =	PD_UPC1_GPIO7	OUT 54 56
RF374 1/20W	1 5% 2 MF 100K 201	PD_UPC1_GPIO9	MAKE_BASE=TRUE =	PD_UPC1_GPIO9	OUT 54 56
RF375 1/20W	1 5% 2 MF 100K 201	PD_UPC1_GPIO10	MAKE_BASE=TRUE =	PD_UPC1_GPIO10	OUT 54 56

CKPLUS_WAIVE=SINGLE_NODENET
on all nets above.

Unused ports

RF316 1/20W	1 5% 2 MF 100K 201	PD_UPC0_DBG6_R	MAKE_BASE=TRUE =	PD_UPC0_DBG6_R	BI 55
RF317 1/20W	1 5% 2 MF 100K 201	PD_UPC0_DBG7_R	MAKE_BASE=TRUE =	PD_UPC0_DBG7_R	BI 55
RF31A 1/20W	1 5% 2 MF 100K 201	PD_UPC0_USBP3_RP	MAKE_BASE=TRUE =	PD_UPC0_USBP3_RP	BI 55
RF31B 1/20W	1 5% 2 MF 100K 201	PD_UPC0_USBP3_RN	MAKE_BASE=TRUE =	PD_UPC0_USBP3_RN	BI 55
RF326 1/20W	1 5% 2 MF 100K 201	PD_UPC1_DBG6_R	MAKE_BASE=TRUE =	PD_UPC1_DBG6_R	BI 56
RF327 1/20W	1 5% 2 MF 100K 201	PD_UPC1_DBG7_R	MAKE_BASE=TRUE =	PD_UPC1_DBG7_R	BI 56
RF32A 1/20W	1 5% 2 MF 100K 201	PD_UPC1_USBP3_RP	MAKE_BASE=TRUE =	PD_UPC1_USBP3_RP	BI 56
RF32B 1/20W	1 5% 2 MF 100K 201	PD_UPC1_USBP3_RN	MAKE_BASE=TRUE =	PD_UPC1_USBP3_RN	BI 56

Connections for Laptops (USBC power in)

PACK_OPTION=USBC_LAPTOP

55	OUT	PP3V3_UPC0_LDO	MAKE_BASE=TRUE	PP3V3_UPC0_LDO	IN 53 55
55	BI	USBC0_CC1	MAKE_BASE=TRUE	USBC0_CC1	BI 55 57
55	BI	USBC0_CC2	MAKE_BASE=TRUE	USBC0_CC2	BI 55 57
56	OUT	PP3V3_UPC1_LDO	MAKE_BASE=TRUE	PP3V3_UPC1_LDO	IN 53 56
56	BI	USBC1_CC1	MAKE_BASE=TRUE	USBC1_CC1	BI 56 57
56	BI	USBC1_CC2	MAKE_BASE=TRUE	USBC1_CC2	BI 56 57

BOM_COST_GROUP=USB-C

SYNC_MASTER=ref_usbc_ace2 SYNC_DATE=05/31/2019

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Apple Inc.

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** OK2INTEGRATE **

PP3V3_UPC0_LDO 53 54 55

Internal Pull-ups
Enabled after reading straps

1M RF409 I2C_UPC0_ATCRTMR0_SCL 51 53 55 58
5% 1/20W MF 201 CKPLUS_WAIVE=I2C_PULLUP

1M RF408 I2C_UPC0_ATCRTMR0_SDA 51 53 55 58
5% 1/20W MF 201 CKPLUS_WAIVE=I2C_PULLUP

10K RF407 INT_I2C_UPC0_ATCRTMR0_L 53 55
5% 1/20W MF 201

1M RF405 UART_UPC01_RX 53 55
5% 1/20W MF 201

100K RF406 PD_UPC0_MRESET 55
5% 1/20W MF 201

100K RF402 PD_UPC0_GPIO5 55
5% 1/20W MF 201

Either a Testpoint or Arkanoid connector
must be present for GPIO0
(EVEN IN PRODUCTION)

CRITICAL
RF403 15K 0.1% 1/20W TF-LF 0201

GND_I2C_ADDR
PRIMARY ONLY

REAR PORT:
CONNECT UPC SPI TO ROM
FRONT PORT:
GROUND UPC SPI

53 PPHV_INT0_AONSW

MAX 100uF TOTAL ON RAIL

79 56 PP5V_S2

79 56 PP5V_S2

CAP FOR PP_5V0 ON VR PAGE

PP_5V0 PP_CABLE PP_HV VBUS

UF400
CD3217B12BCE
FCBGA

353S02158
CRITICAL
OMIT_TABLE

		B13	HRESET		
55	PD_UPC0_MRESET	A14	MRESET		
58 53 51	ATCRTMR0_RESET_L	B17	RESET*		
53	UPC0_SER_DBG	A2	GPIO0		
		B1			
53	FLASH_BUSY_USBC01_L	D1	GPIO1		
55 53	INT_I2C_UPC0_ATCRTMR0_L	F1	GPIO2		
53	UPC0_5V_EN	C2	GPIO3		
53 51	ATCRTMR0_FORCE_PWR	E2	GPIO4		
54	PD_UPC0_GPIO5	B3	GPIO5		
59 55	UPC_FORCE_PWR	C4	GPIO6	DIGITAL CORE I/O & CONTROL	
54	SOC_DOCK_CONNECT	D3	GPIO7		
56 35	UPC_PMU_RESET_3V3	E4	GPIO8		
54	SOC_DFU_STATUS	F3	GPIO9		
54	SOC_FORCE_DFU	F7	GPIO10		
54	PP3V3_UPC0_LDO	A18	BUSPOWER		
53	GND	M19	I2C_ADDR	IPU-BOOT	
	UPC0_R_OSC	M21	R_OSC		
58 55 53 51	I2C_UPC0_ATCRTMR0_SDA	A16	I2CM_SDA_CNFG		
58 55 53 51	I2C_UPC0_ATCRTMR0_SCL	B15	I2CM_SCL_CNFG		
53 43	I2C_UPC_SDA	B5	I2C_SDA1		
53 43	I2C_UPC_SCL	A4	I2C_SCL1		
53 41	UPC_I2C_INT_L	D7	I2C_IRQ1*		
53 43	I2C_SMC_UPC_SDA	B7	I2C_SDA2		
53 43	I2C_SMC_UPC_SCL	A6	I2C_SCL2		
53 43	UPC_SMC_I2C_INT_L	C8	I2C_IRQ2*		
53	SPI_UPC01_R_CLK	B9	SPI_CLK		
53	SPI_UPC01_R_MOSI	B11	SPI_MOSI		
53	SPI_UPC01_R_MISO	A10	SPI_MISO		
53	SPI_UPC01_R_CS_L	A8	SPI_SSZ		
53	SWD_UPC_SWDIO0	E20	SWD_DATA	IPU	
53	SWD_UPC_SWCLK	E16	SWD_CLK	IPU	
55 53	UART_UPC01_RX	B19	UART_RX		
53	UART_UPC01_TX	A20	UART_TX		
59	USB2_UPC0_P1_P	H19	USB_RP1_P		
59	USB2_UPC0_P1_N	H21	USB_RP1_N		
54	USB_DBG_LS_P	G20	USB_RP2_P		
54	USB_DBG_LS_N	G22	USB_RP2_N	PORT_MUX	
54	PD_UPC0_USBP3_RP	F19	USB_RP3_P		
54	PD_UPC0_USBP3_RN	F21	USB_RP3_N		
53	USBC0_AUXLSX_P	J12	AUX_P		
53	USBC0_AUXLSX_N	H11	AUX_N		
53	ROM_UPC01_WP_L	C12	HPD		
54	UART_DEBUGPRT_R2D	G12	DEBUG0		
54	UART_DEBUGPRT_D2R	F11	DEBUG1		
54	SWD_SOC_SWCLK	E8	DEBUG2		
54	SWD_SOC_SWDIO	E12	DEBUG3		
54	UART_SMC_DEBUGPRT_R2D	G16	DEBUG4		
54	UART_SMC_DEBUGPRT_D2R	F15	DEBUG5		
54	PD_UPC0_DBG6_R	D15	DEBUG6		
54	PD_UPC0_DBG7_R	D19	DEBUG7		

VIN_3V3	C20		
VDDIO	A12		
VDDIO_CFG	D11	GND	53
LDO_3V3	C22		
	D21		
VIN_LV	L20		
VOUT_LV	L18		
VRET	C16		
SS	L22	UPC0_SS	
LDO_CORE	E22	PP1V5_UPC0_LDO_CORE	
VBUS_OPT	D5	PPVBUS_USBC0	53
PP_HV_OPT	F5	PPHV_INT0_AONSW	53
C_CC1	M15	USBC0_CC1	
	N16		
C_CC2	M17	USBC0_CC2	
	N18		
RPD_G1	L14	USBC0_CC1	BI 54
RPD_G2	L16	USBC0_CC2	BI 54
C_USB_TP	K19	USBC0_USB_TOP_P	BI 57
C_USB_TN	K21	USBC0_USB_TOP_N	BI 57
C_USB_BP	J20	USBC0_USB_BOT_P	BI 57
C_USB_BN	J22	USBC0_USB_BOT_N	BI 57
C_SBU1	J16	USBC0_SBU1	BI 57
C_SBU2	H15	USBC0_SBU2	BI 57
GND_OPT	C18		
GND_OPT	E18		
GND_OPT	D17		
GND_OPT	G18		

POWER

TYPE-C

GND

PPVBUS_USBC0 53 57

CF401 1UF 10% 35V X5R 0402

PP3V3_S2_UPC 53 56 78

CF400 10UF 20% 6.3V CERM 0402

PP1V25_S2 53 56 78

CF402 1.0UF 20% 6.3V X5R 0201-1

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V

PP3V3_UPC0_LDO 53 54 55

CF408 10UF 20% 6.3V CERM 0402

PP1V8_S2 54 58

CF403 0.1UF 10% 6.3V CERM-XSR 0201

USBC0_3V3LDO_EN 59

(cap needed when used as power source)

PACK_OPTION=ACE2_SS_CAP

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750

CF405 10UF 20% 6.3V CERM 0402

CF409 0.68UF 5% 6.3V X6S 0402

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500

BI 54 57

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500

BI 54 57

CF414 220PF 5% 50V C0G 0201-1

CF413 220PF 5% 50V C0G 0201-1

GND

A22 H9 K20 B21 K15 K22

BOM_COST_GROUP=USB-C

SYNC_MASTER=rsf_usbc_mcd2 SYNC_DATE=05/31/2019

PAGE TITLE

USB-C: Port Controller ATC0

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PP3V3_UPC1_LDO 53 54 56

1M RF509 I2C_UPC1_ATCRTMR1_SCL 52 53 56 58
5% 1/20W MF 201 CKPLUS_WAIVE=I2C_PULLUP

1M RF508 I2C_UPC1_ATCRTMR1_SDA 52 53 56 58
5% 1/20W MF 201 CKPLUS_WAIVE=I2C_PULLUP

10K RF507 INT_I2C_UPC1_ATCRTMR1_L 53 56
5% 1/20W MF 201

1M RF505 UART_UPC01_TX 53 56
5% 1/20W MF 201

100K RF506 PD_UPC1_MRESET 56
5% 1/20W MF 201

100K RF502 PD_UPC1_GPIO5 56
5% 1/20W MF 201

Either a Testpoint or Arkanoid connector
must be present for GPIO0
(EVEN IN PRODUCTION)

CRITICAL
RF503 15K 0.1% 1/20W TF-LF 0201

GND/I2C_ADDR
PRIMARY ONLY

REAR PORT:
CONNECT UPC SPI TO ROM
FRONT PORT:
GROUND UPC SPI

53 PPHV_INT1_AONSW

MAX 100uF TOTAL ON RAIL

79 55 PP5V_S2

79 55 PP5V_S2

CAP FOR PP_5V0 ON VR PAGE

K9 L10 M9 N10 K11 L12 M11 N12 — PP_5V0
N14 — PP_CABLE
M13 G2 G4 H1 H3 J2 J4 K1 K3 L2 L4 M1 M3 N2 N4 — PP_HV
G6 G8 H5 H7 J6 J8 K5 K7 L6 L8 M5 M7 N6 N8 — VBUS

UF500
CD3217B12BCE
FCBGA

353S02158
CRITICAL
OMIT_TABLE

			B13	HRESET	
56		PD_UPC1_MRESET	A14	MRESET	
58 52	OUT	ATCRTMR1_RESET_L	B17	RESET*	
53	OUT	UPC1_SER_DBG	A2	GPIO0	
			B1		
53	OUT	PD_UPC1_GPIO1	D1	GPIO1	
56 53	IN	INT_I2C_UPC1_ATCRTMR1_L	F1	GPIO2	
53	OUT	UPC1_5V_EN	C2	GPIO3	
53 52	OUT	ATCRTMR1_FORCE_PWR	E2	GPIO4	
56	OUT	PD_UPC1_GPIO5	B3	GPIO5	
59 56	IN	UPC_FORCE_PWR	C4	GPIO6	DIGITAL CORE I/O & CONTROL
54	OUT	PD_UPC1_GPIO7	D3	GPIO7	
55 35	OUT	UPC_PMU_RESET_3V3	E4	GPIO8	
54	IN	PD_UPC1_GPIO9	F3	GPIO9	
54	OUT	PD_UPC1_GPIO10	F7	GPIO10	
54		PP3V3_UPC1_LDO	A18	BUSPOWER	
53		NC_UPC1_I2C_ADDR	M19	I2C_ADDR	IPU-BOOT
		UPC1_R_OSC	M21	R_OSC	
58 56 53 52	BI	I2C_UPC1_ATCRTMR1_SDA	A16	I2CM_SDA_CNFG	
58 56 53 52	BI	I2C_UPC1_ATCRTMR1_SCL	B15	I2CM_SCL_CNFG	
41	BI	I2C_UPC_SDA	B5	I2C_SDA1	
41	BI	I2C_UPC_SCL	A4	I2C_SCL1	
41	OUT	UPC_I2C_INT_L	D7	I2C_IRQ1*	
43	BI	I2C_SMC_UPC_SDA	B7	I2C_SDA2	
43	BI	I2C_SMC_UPC_SCL	A6	I2C_SCL2	
43	OUT	UPC_SMC_I2C_INT_L	C8	I2C_IRQ2*	
		GND	B9	SPI_CLK	
53	OUT	GND	B11	SPI_MOSI	
53	OUT	GND	A10	SPI_MISO	
53	IN	GND	A8	SPI_SSZ	
53	BI	SWD_UPC01_UART_DATA	E20	SWD_DATA	IPU
53	BI	SWD_UPC01_UART_CLK	E16	SWD_CLK	IPU
56 53	IN	UART_UPC01_TX	B19	UART_RX	
53	OUT	UART_UPC01_RX	A20	UART_TX	
59	BI	USB2_UPC1_P1_P	H19	USB_RP1_P	
59	BI	USB2_UPC1_P1_N	H21	USB_RP1_N	
54	BI	PD_UPC1_USBP2_RP	G20	USB_RP2_P	
54	BI	PD_UPC1_USBP2_RN	G22	USB_RP2_N	
54	BI	PD_UPC1_USBP3_RP	F19	USB_RP3_P	
54	BI	PD_UPC1_USBP3_RN	F21	USB_RP3_N	
52	BI	USBC1_AUXLSX_P	J12	AUX_P	
52	BI	USBC1_AUXLSX_N	H11	AUX_N	
53	OUT	PD_UPC1_HPD	C12	HPD	
54	BI	PD_UPC1_DBG0_R	G12	DEBUG0	
54	BI	PD_UPC1_DBG1_R	F11	DEBUG1	
54	OUT	PD_UPC1_DBG2_R	E8	DEBUG2	
54	BI	PD_UPC1_DBG3_R	E12	DEBUG3	
54	BI	PD_UPC1_DBG4_R	G16	DEBUG4	
54	BI	PD_UPC1_DBG5_R	F15	DEBUG5	
54	IN	PD_UPC1_DBG6_R	D15	DEBUG6	
54	OUT	PD_UPC1_DBG7_R	D19	DEBUG7	

PORT_MUX

POWER

TYPE-C

GND

VIN_3V3	C20		
VDDIO	A12		
VDDIO_CFG	D11	GND	53
LDO_3V3	C22		
	D21		
VIN_LV	L20		
VOUT_LV	L18		
VRET	C16		
SS	L22	UPC1_SS	
LDO_CORE	E22	PP1V5_UPC1_LDO_CORE	
VBUS_OPT	D5	PPVBUS_USBC1	53
PP_HV_OPT	F5	PPHV_INT1_AONSW	53
C_CC1	M15	USBC1_CC1	
	N16		
C_CC2	M17	USBC1_CC2	
	N18		
RPD_G1	L14	USBC1_CC1	BI 54
RPD_G2	L16	USBC1_CC2	BI 54
C_USB_TP	K19	USBC1_USB_TOP_P	BI 57
C_USB_TN	K21	USBC1_USB_TOP_N	BI 57
C_USB_BP	J20	USBC1_USB_BOT_P	BI 57
C_USB_BN	J22	USBC1_USB_BOT_N	BI 57
C_SBU1	J16	USBC1_SBU1	BI 57
C_SBU2	H15	USBC1_SBU2	BI 57

PPVBUS_USBC1 53 57

CF501 1UF 10% 25V X5R 0402

PP3V3_S2_UPC 53 55 78

CF500 10UF 20% 6.3V CERM 0402

PP1V25_S2 53 55 78

CF502 1.0UF 20% 6.3V X5R 0201-1

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V

PP3V3_UPC1_LDO 53 54 56

CF508 10UF 20% 6.3V CERM 0402

PP1V8_S2 54 58

CF503 0.1UF 10% 6.3V CERM-X5R 0201

USBC1_3V3LDO_EN 59

(cap needed when used as power source)

PACK_OPTION=ACE2_SS_CAP

CF509 0.68UF 5% 6.3V X6S 0402

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750

CF505 10UF 20% 6.3V CERM 0402

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500

BI 54 57

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500

BI 54 57

CF514 220PF 5% 50V C0G 0201-1

CF513 220PF 5% 50V C0G 0201-1

GND_OPT C18
GND_OPT E18
GND_OPT D17
GND_OPT G18

GND

A22 H9 N20 R21 K15 N22

BOM_COST_GROUP=USB-C

SYNC_MASTER=ref_usbc_ace2 SYNC_DATE=05/31/2019

PAGE TITLE
USB-C: Port Controller ATC1

Apple Inc.

DRAWING NUMBER 051-05392 SIZE D
REVISION 4.0.0
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SHEET 56 OF 92

---- Reference only ----

Left Rear Port

FOR POR, VERIFY 20% TOLERANCE ON 0.22UF AC COUPLING CAP IS OK

PLACE VBUS CAP NEAR EACH VBUS PIN

516S00457
Mates with:
x on y
(NO LANE REVERSALS ALLOWED)

JF600
20875-056E-01
F-ST-SM

PPVBUS_USBC0
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=20V

TPT_USBC0_PP20V — TP-P4 — TPF600

TPT_USBC1_PP20V — TP-P4 — TPF601

USBC0 CC1 / USBC0 CC2

USBC0 R2D CR N<1> / USBC0 R2D CR P<1> / USBC0 R2D CR N<2> / USBC0 R2D CR P<2>

USBC0 R2D C N<1> / USBC0 R2D C P<1> / USBC0 R2D C N<2> / USBC0 R2D C P<2>

USBC0 R2D N<1> / USBC0 R2D P<1> / USBC0 R2D N<2> / USBC0 R2D P<2>

USBC0 D2R CR N<1> / USBC0 D2R CR P<1> / USBC0 D2R CR N<2> / USBC0 D2R CR P<2>

USBC0 D2R C N<1> / USBC0 D2R C P<1> / USBC0 D2R C N<2> / USBC0 D2R C P<2>

USBC0 D2R N<1> / USBC0 D2R P<1> / USBC0 D2R N<2> / USBC0 D2R P<2>

USBC0 SBU2 / USBC0 SBU1

USBC0 USB BOT N / USBC0 USB BOT P

USBC0 USB TOP P / USBC0 USB TOP N

USBC1 SBU2 / USBC1 SBU1

USBC1 USB BOT N / USBC1 USB BOT P

USBC1 USB TOP P / USBC1 USB TOP N

USBC1 R2D CR P<2> / USBC1 R2D CR N<2> / USBC1 R2D CR P<1> / USBC1 R2D CR N<1>

USBC1 R2D C P<2> / USBC1 R2D C N<2> / USBC1 R2D C P<1> / USBC1 R2D C N<1>

USBC1 R2D P<2> / USBC1 R2D N<2> / USBC1 R2D P<1> / USBC1 R2D N<1>

USBC1 D2R P<2> / USBC1 D2R N<2> / USBC1 D2R CR P<1> / USBC1 D2R CR N<1>

USBC1 D2R C P<2> / USBC1 D2R C N<2> / USBC1 D2R C P<1> / USBC1 D2R C N<1>

USBC1 D2R P<2> / USBC1 D2R N<2> / USBC1 D2R P<1> / USBC1 D2R N<1>

USBC1 CC2 / USBC1 CC1

DF622 TVS2200 WSON — PLACE_NEAR=JF600.58:5MM — ALLOW_APPLE_PREFIX=D

DF602 TVS2200 WSON — PLACE_NEAR=JF600.59:5MM — ALLOW_APPLE_PREFIX=D

JDZF620 X3-WLB1608-1 SDM2U40CSP

DZF600 X3-WLB1608-1 SDM2U40CSP

PPVBUS_USBC1
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=20V

FOR POR, VERIFY 20% TOLERANCE ON 0.22UF AC COUPLING CAP IS OK

PLACE VBUS CAP NEAR EACH VBUS PIN

Cowling Bosses

860-01443

SHF600 3.10D1.65ID-1.12H-SM — ALLOW_APPLE_PREFIX=SH

SHF601 3.10D1.65ID-1.12H-SM — ALLOW_APPLE_PREFIX=SH

BOM_COST_GROUP=USB-C

Left Front Port

SYNC_MASTER=ref_usbc_acs2 — SYNC_DATE=05/31/2019

PAGE TITLE: USB-C: Connector(s)

Apple Inc.

DRAWING NUMBER: 051-05392 — SIZE: D

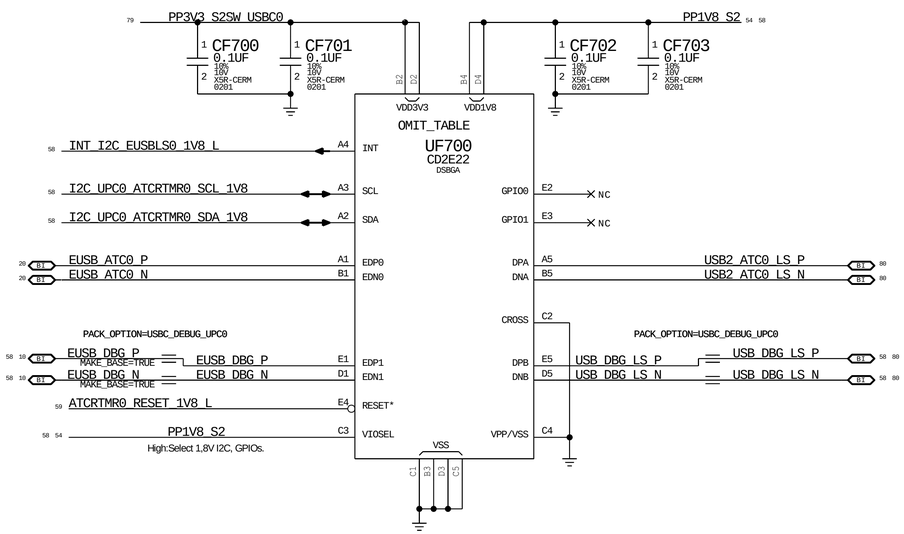
REVISION: 4.0.0

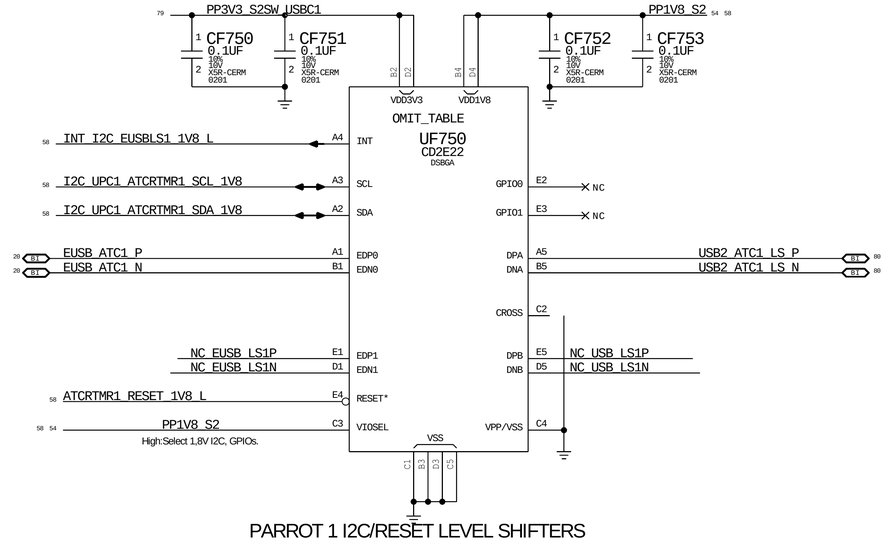
BRANCH: evt-1

PAGE: 156 OF 801

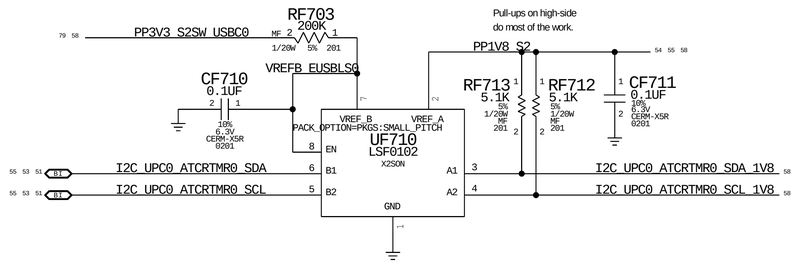
SHEET: 57 OF 92

** OK2INTEGRATE **





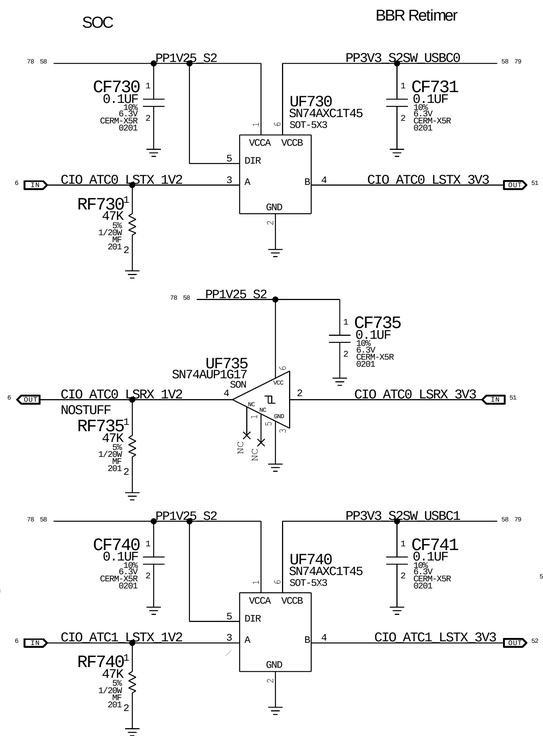
PARROT 0 I2C/RESET LEVEL SHIFTERS



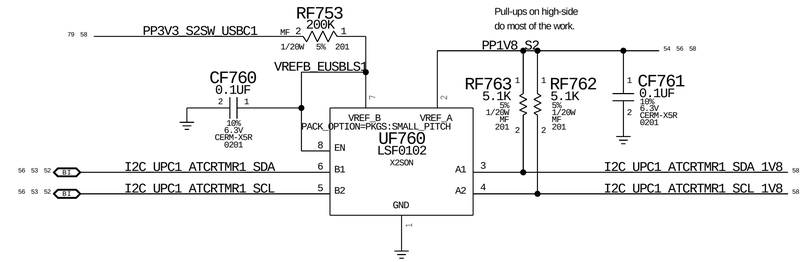
TBT LS RX/TX LEVEL SHIFTERS

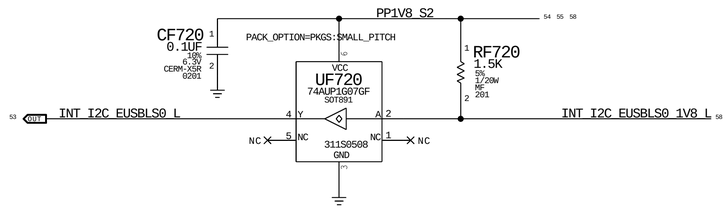
SOC

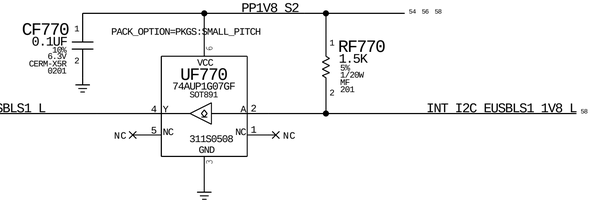
BBR Retimer

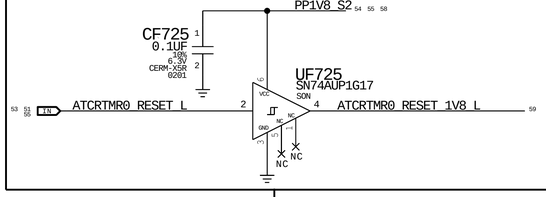


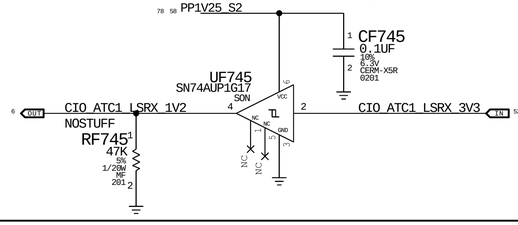
PARROT 1 I2C/RESET LEVEL SHIFTERS

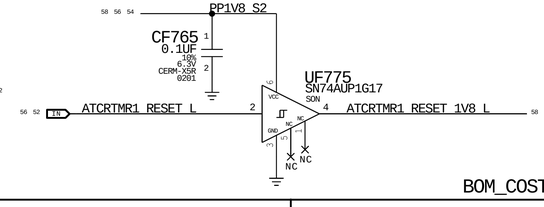












BOM_COST_GROUP=USB-C

SYNC_MASTER=ref_usbc_mlb2 SYNC_DATE=05/31/2019

PAGE TITLE

USB-C: HS Level Shifters

Apple Inc.

DRAWING NUMBER 051-05392 SIZE D

REVISION 4.0.0

BRANCH evt-1

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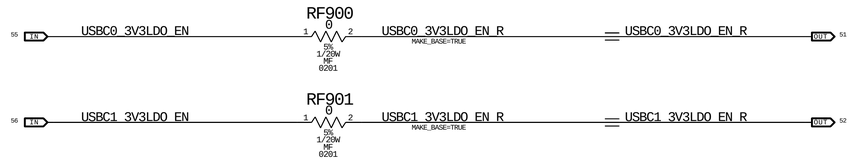
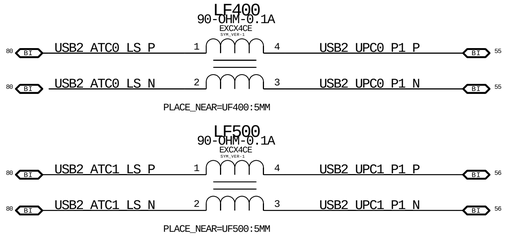
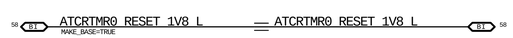
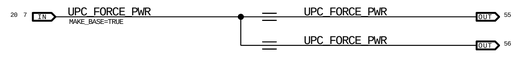




Alias Debug Reset signal to ATC0 Debug Level Shifter (UF700)



Tie ACE2 Pin C4 (GPIO6) together and alias to UPC_FORCE_PWR.



SYNC_MASTER=vf_usbc_ace2
SYNC_DATE=05/31/2019

PAGE TITLE
USB-C: Project Specific

Apple Inc.

DRAWING NUMBER 051-05392
SIZE D
REVISION 4.0.0
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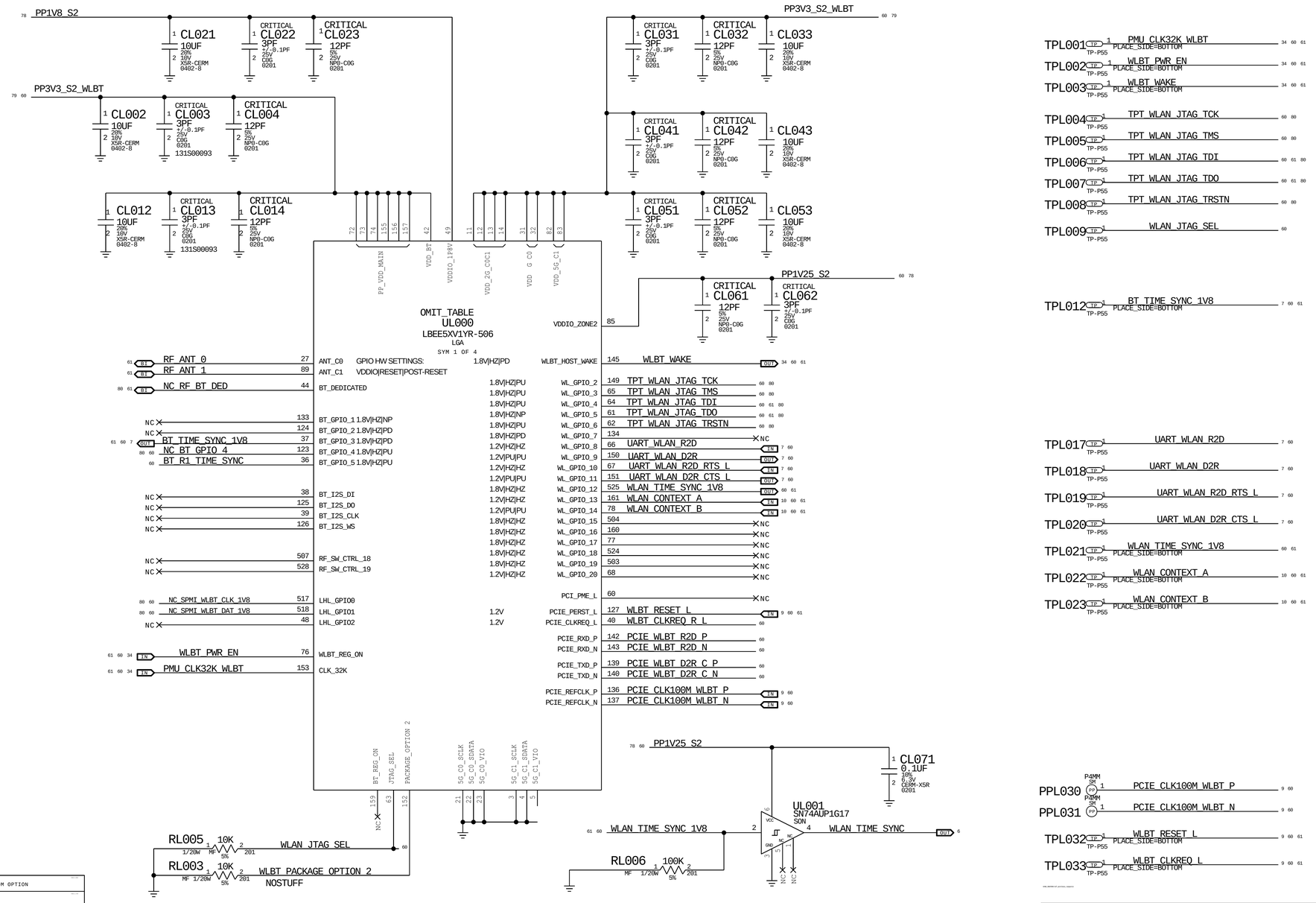
*** OK2INTEGRATE ***

RASPUTIN WIFI/BT MODULE

FOR HOSTINTERFACE TABLES REFER TO:
RDAR://PROBLEM/53187294

FOR DESIGN DOCUMENTATION,
SYSTEM INTEGRATION QUESTIONS:
RDAR://PROBLEM/44786407



RASPUTIN BOM TABLE:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00763	1	MODULE, WLAN BT, RASPUTIN, ES6.11, M, LGA49	UL000	CRITICAL	

RASPUTIN ALTERNATE BOM:

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00758	339S00763	ANY	UL000	RASPUTIN USI ES6.5

BOM_COST_GROUP=WIRELESS

SYNC_MASTER=ref_ustc_dcc2 SYNC_DATE=05/31/2019

PAGE TITLE: WIFI/BT: MODULE

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D
REVISION: 4.0.0
BRANCH: evt-1
PAGE: 200 OF 801
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*** OK2INTEGRATE ***

RASPUTIN WIFI/BT MODULE GND

OMIT_TABLE

UL000
LBEE5XV1YR-506
LGA
SYM 2 OF 4

1		119	
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58	GND	179	GND
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OMIT_TABLE

UL000
LBEE5XV1YR-506
LGA
SYM 3 OF 4

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256		337	
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302		383	

OMIT_TABLE

UL000
LBEE5XV1YR-506
LGA
SYM 4 OF 4

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436		520	
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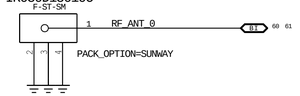
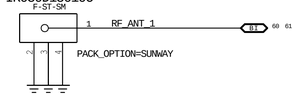
438		522	
439		523	
440		526	
441		527	
442		529	
443		530	
444		531	
445		532	
446		533	
447		534	
448		535	
449		536	
450		537	
451		538	
452		539	
453		540	
454		541	
455		542	
456		543	
457		544	
458		545	
459		546	
460		547	
461		548	
462		549	

ANTENNA CONNECTORS

JL100
IR050D15010C
F-ST-SM

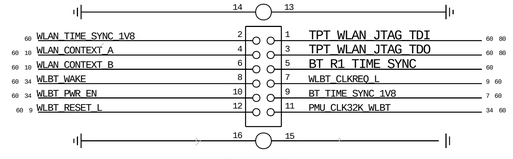


JL101
IR050D15010C
F-ST-SM



WLBT DEBUG CONNECTOR

JL103
505070-1222
M-ST-SM



BOMOPTION=WLBT_DBG
PACK_OPTION=WLBT_DBG_CONN

SYNC_MASTER=ref_usbc_acc2 SYNC_DATE=05/31/2019

PAGE TITLE
WIFI/BT: ANTENNA and GND

Apple Inc.

DRAWING NUMBER 051-05392 SIZE D
REVISION 4.0.0
BRANCH evt-1
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*** OK2INTEGRATE ***

NAND0 S5E0

PP0V88_AWAKE_NAND
CN010 20UF 20% 10V X5R 0402
CN011 20UF 20% 10V X5R 0402
CN012 2.2UF 20% 10V X5R 0201
CN013 2.2UF 20% 10V X5R 0201
CN014 2.2UF 20% 10V X5R 0201
CN015 0.1UF 10% 6.3V CERM-X5R 0201
CN016 0.1UF 10% 6.3V CERM-X5R 0201
CN017 0.1UF 10% 6.3V CERM-X5R 0201

PP1V25_AWAKE_NAND
CN032 20UF 20% 10V X5R 0402
CN030 4.3UF 20% 4V CERM 0402
CN034 2.2UF 20% 10V X5R 0201
CN035 2.2UF 20% 10V X5R 0201
CN036 2.2UF 20% 10V X5R 0201
CN037 2.2UF 20% 10V X5R 0201
CN038 2.2UF 20% 10V X5R 0201
CN039 2.2UF 20% 10V X5R 0201
CN03A 2.2UF 20% 10V X5R 0201

PP2V5_AWAKE_NAND
CN020 20UF 20% 10V X5R 0402
CN022 2.2UF 20% 10V X5R 0201
CN023 2.2UF 20% 10V X5R 0201
CN024 2.2UF 20% 10V X5R 0201
CN025 2.2UF 20% 10V X5R 0201

TPT_NAND0_S5E0_ANI1_VREF
TPT_NAND0_S5E0_ANI0_VREF

PP1V25_AWAKE_NAND
RN010 2 1% 1/20W MF 0201 PLACE_NEAR=UN000.L2:10MM
CN047 2.2UF 20% 10V X5R 0201
CN046 0.1UF 10% 6.3V CERM-X5R 0201
MIN_LINE_WIDTH=0.1000 MIN_NECK_WIDTH=0.1000 VOLTAGE=1.2V
PP1V2_NAND0_S5E0_AVDD1X_PLL

FLN000 10OHM-50%-1A-0.050OHM 0201 PLACE_NEAR=UN000.J6:10MM
CN045 4.7UF 20% 4V CER-X5R 0201
CN044 0.1UF 10% 6.3V CERM-X5R 0201
MIN_LINE_WIDTH=0.1000 MIN_NECK_WIDTH=0.1000 VOLTAGE=1.2V
PP1V2_NAND0_S5E0_PCI_AVDD_H

The inductance from CN047, CN046, CN045, CN044 to their S5E pins shall be less than 1100pH

MIN_LINE_WIDTH=0.1000 MIN_NECK_WIDTH=0.1000 VOLTAGE=0.9V
PP0V9_NAND0_S5E0_VDD_PLL
NC_NAND0_S5E0_VPP

FLN001 10OHM-50%-1A-0.050OHM 0201 PLACE_NEAR=UN000.R4:10MM
PP0V88_AWAKE_NAND
CN083 4.7UF 20% 4V CER-X5R 0201 PLACE_NEAR=FLN001.2:5MM

J6 PCIE_AVDD_H
J8 PCIE_VDD
K9 PCIE_VDD
N6 PCIE_VDD
N8 PCIE_VDD
L2 AVDD1X_PLL
G12 ANIO_VREF
J4 ANI1_VREF
G6 G8 L6 L8 R6 R8 VDD
J2 VDDIO_1
K9 T5 VDDIO_1
E10 E2 N2 P9 VDDIO_2
D3 VCC
E12 G4 L12 R2 VCC
R4 VDD_PLL
F3 VPP
F5 VQPS

CN085 10PF 5% 25V C0G 0201
RN004 200 0.1% 1/20W TK 0201-1
CN003 0.22UF 10% 6.3V X5R-CERM 0201
CN004 0.22UF 10% 6.3V X5R-CERM 0201
CN001 0.22UF 10% 6.3V X5R-CERM 0201
CN002 0.22UF 10% 6.3V X5R-CERM 0201
GND_VOID=TRUE

NAND0_CLK24M_0 → M3 CLK_IN
PCIE_CLK100M_NAND0_0_P → K11 PCIE_REFCLK_P
PCIE_CLK100M_NAND0_0_N → J12 PCIE_REFCLK_N
NAND0_CLKREQ0_R_L ← P5 PCIE_CLKREQ*
NAND0_S5E0_PCIE_RESREF → H7 PCIE_RESREF
PCIE_NAND0_R2D_C_P<0> → PCIE_NAND0_R2D_P<0> → M11 PCIE_RX0_P
PCIE_NAND0_R2D_C_N<0> → PCIE_NAND0_R2D_N<0> → N12 PCIE_RX0_N
PCIE_NAND0_D2R_P<0> ← PCIE_NAND0_D2R_C_P<0> ← R12 PCIE_TX0_P
PCIE_NAND0_D2R_N<0> ← PCIE_NAND0_D2R_C_N<0> ← T11 PCIE_TX0_N

OMIT_TABLE
UN000
S5E-MCP-STUDY
LGA

NAND0_RESET_L → L4 RESET*
NAND0_JTAG_TRST_L → G10 TRST*
NAND0_S5E0_ZQ_0 → C10 ZQ_0
NAND0_S5E0_ZQ_1 → K3 ZQ_1

RN006 300 1% 1/20W MF 201 PLACE_NEAR=UN000.C10:15MM
RN005 300 1% 1/20W MF 201 PLACE_NEAR=UN000.K3:15MM

A12 A2 B1 B13 C12 C2 D1 D13 F1 F13 F7 F9 H1 H13 H3 H5 H9 J10 K1 K13 K5 K7 L10 M1 M13 M5 M7 N10 N4 P1 P11 P13 P3 P7 R10 T1 T13 T7 T9 U12 U2 VSS

A10 A4 A6 A8 U10 U4 U6 U8 VSS_R

EXT_D0/BOOT0 B3 NAND0_LPB_L
EXT_D1/BOOT1 C4 NAND_BFH
EXT_D2/BOOT2/SPINAND_SCLK B5 NAND0_BOOT2
EXT_D3/SWD_UID0/SPINAND_MISO C6 NAND0_S5E0_SWD_UID0
EXT_D4/SPI_CS B7
EXT_D5/SWD_UID1/SPINAND_MOSI C8 NAND0_S5E0_SWD_UID1
EXT_D6/BOOT3 B9
EXT_D7/SPF B11 NAND0_PFN_L
EXT_DQS/BCM* D11 NAND0_BCM_L
EXT_NCE/PERST* E8 NAND0_PCIE_RESET_L
EXT_NRE/JTAG_TMS D7 SWD_NAND0_SWDIO
EXT_NWE/JTAG_TCK E6 SWD_NAND0_SWCLK
EXT_RNB/JTAG_TDO E4 NAND0_S5E0_JTAG_TDO
EXT_CLE/JTAG_TDI D5 TPT_NAND0_S5E0_JTAG_TDI
EXT_ALE/JTAG_SEL D9 NAND0_JTAG_SEL
DROOP* T3 TPT_NAND0_S5E0_DROOP_L
WP* G2 NAND0_WP_L

NAND0_BOOT2
NAND0_JTAG_SEL
NAND0_JTAG_TRST_L
RN000 47K 1% 1/20W MF 201
RN002 47K 1% 1/20W MF 201
RN021 0 5% 1/20W MF 0201
Spec recommends to tie Boot2 directly to Gnd

PP1V25_AWAKE_NAND
RN001 0 5% 1/20W MF 0201
RN007 0 5% 1/20W MF 0201
NAND0_BCM_L
NAND0_WP_L
Spec recommends to tie BCM, WP directly to 1.2V rail

NAND0_S5E0_SWD_UID0
NAND0_S5E0_SWD_UID1
RN009 47K 1% 1/20W MF 201
RN008 47K 1% 1/20W MF 201
BOM_COST_GROUP=SSD

SYNC_MASTER=ref_storage_s5e
SYNC_DATE=05/31/2019
PAGE TITLE
STORAGE: SSD0 S5E <0>
Apple Inc.
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REVISION 4.0.0
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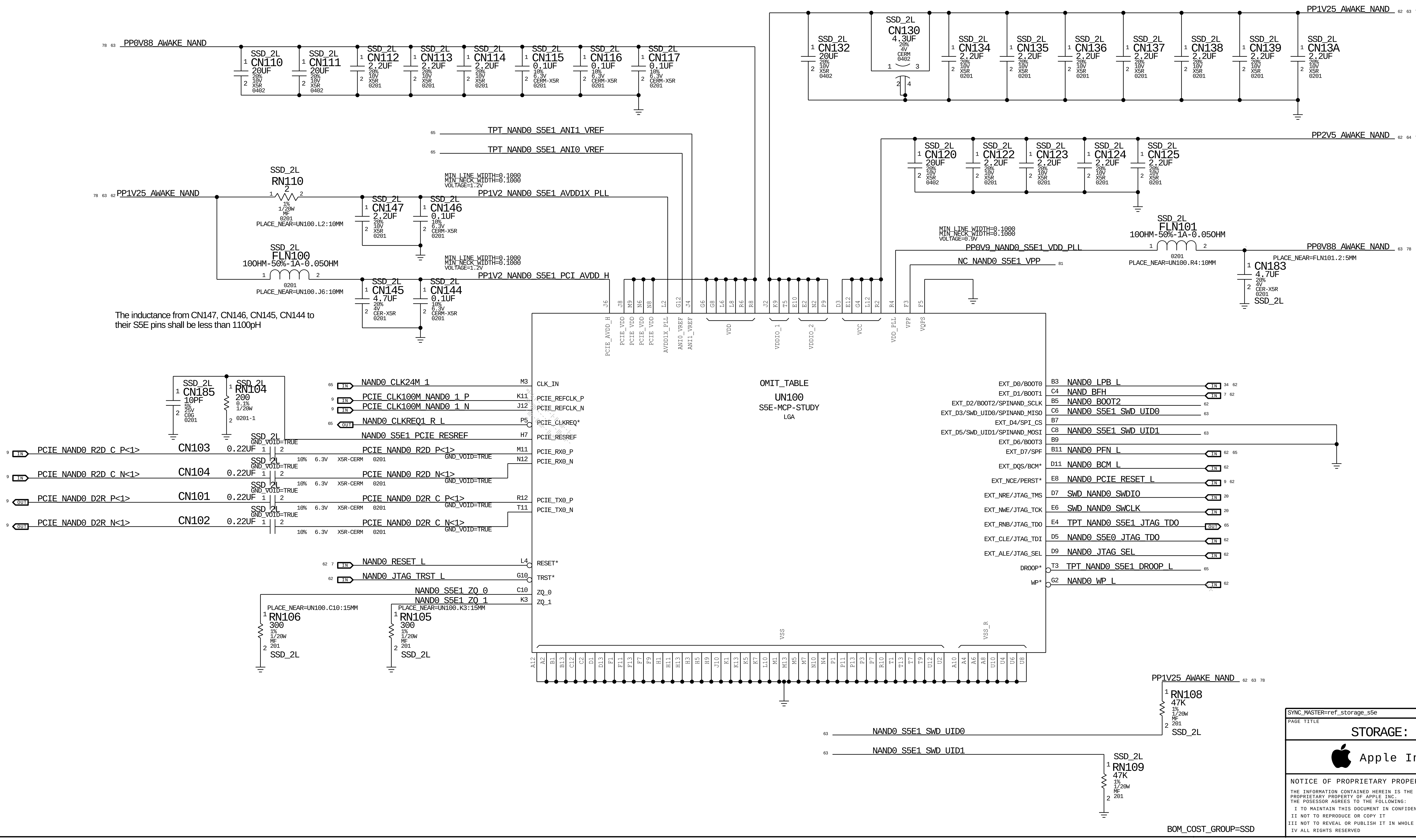
*** OK2INTEGRATE ***

NAND0 S5E1



BOM_COST_GROUP=SSD

SYNC_MASTER=ref_storage_s5e SYNC_DATE=05/31/2019

PAGE TITLE: STORAGE: SSD0 S5E <1>

Apple Inc.

DRAWING NUMBER: 051-05392 SIZE: D

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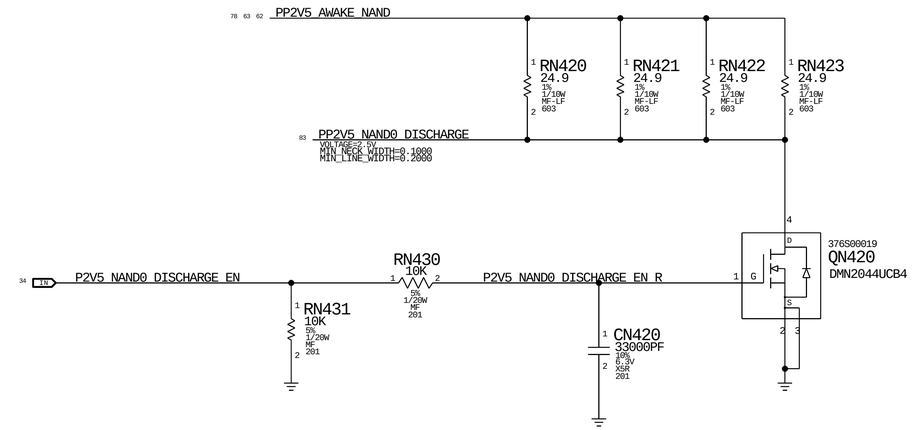
OK2INTEGRATE

THIS EXTERNAL NAND VCC DISCHARGE CIRCUITRY IS FOR SYSTEM THAT DOES NOT USE OCARINA



SYNC_MASTER=ref_storage_s5e SYNC_DATE=05/31/2019

PAGE TITLE

STORAGE: NON OCARINA SUPPORT

Apple Inc.

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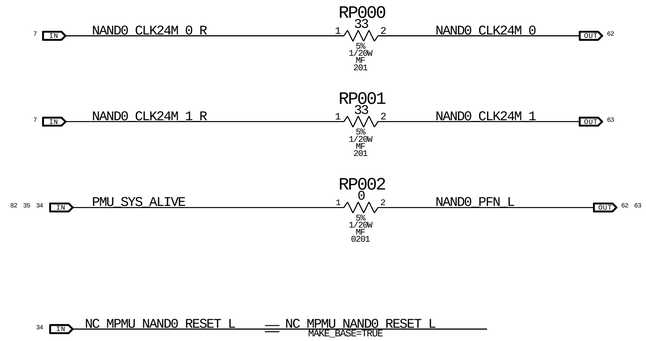
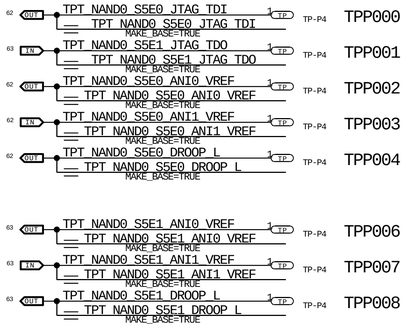
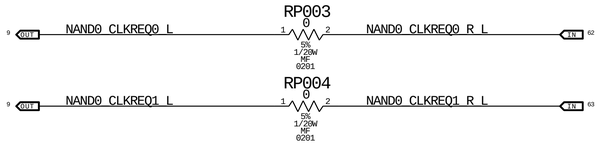
SSD 24M CLOCK TERMINATIONS

TOPOLOGY TBD







SYNC_MASTER=ref_storage_s5e SYNC_DATE=05/31/2019

PAGE TITLE

STORAGE: SSD Support

Apple Inc.

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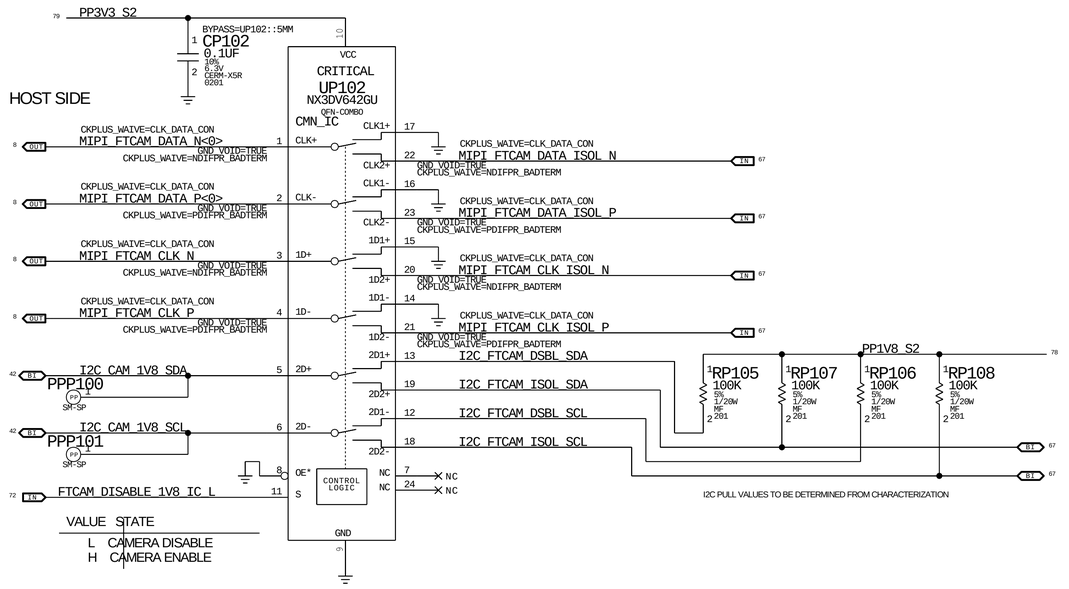
*** OK2INTEGRATE ***

CAMERA SECURE DISABLE
ACTUAL NOT ON THE BOARD



SYNC_MASTER=ref_storage_s5e	SYNC_DATE=05/31/2019
PAGE TITLE	SECDIS: MIPI MUX
Apple Inc.	DRAWING NUMBER 051-05392 · SIZE D
	REVISION 4.0.0
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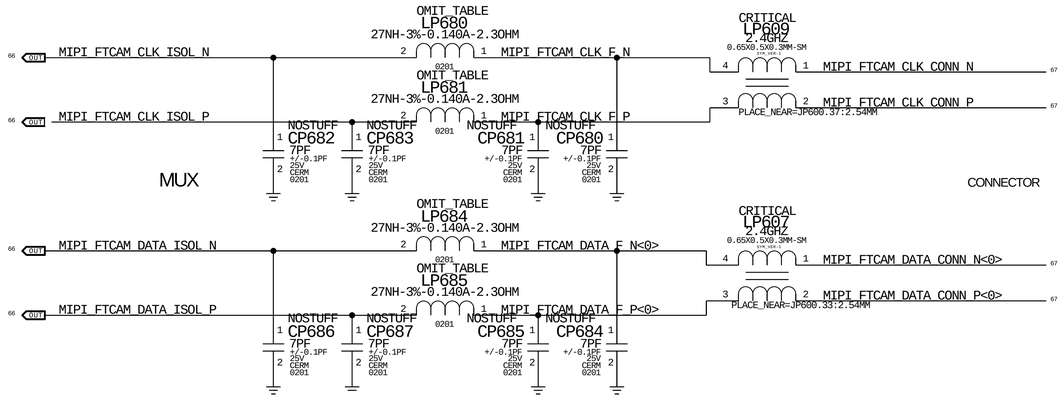
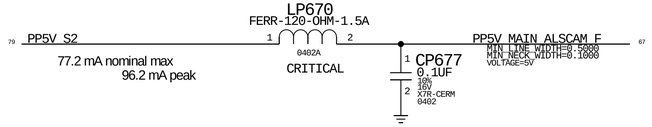
LCD PANEL INTERFACE (eDP) + Camera (MIPI)

A MIPI Clock and Data

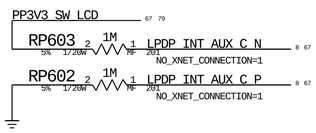
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S0201	4	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	LP680,LP681,LP684,LP685		



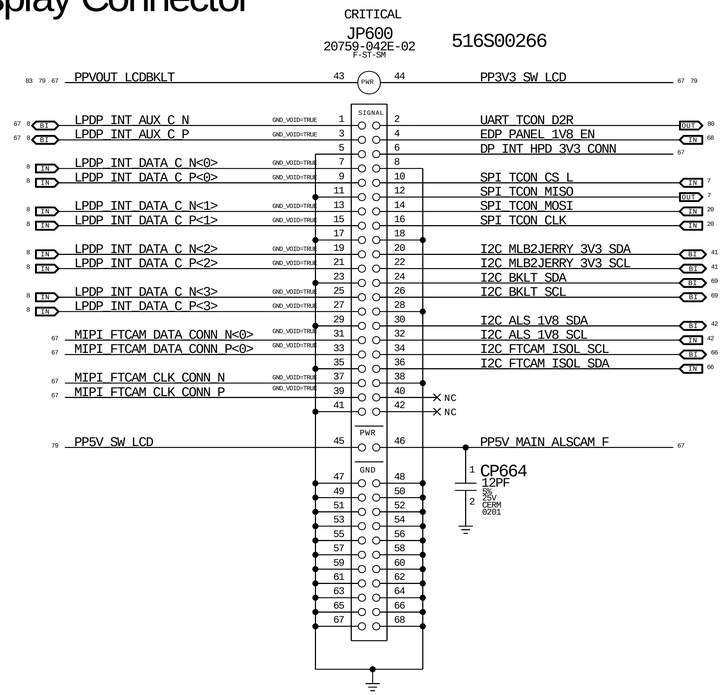
B ALS & Camera 5V Filter



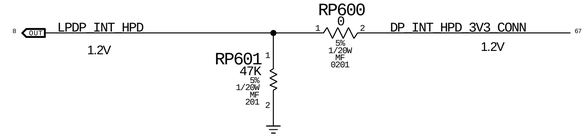
C LCD Panel AUX Straps



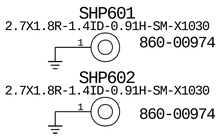
G eDP Display Connector



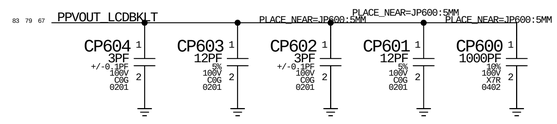
D TCON HPD Voltage Divider



E Cowling Bosses



F Backlight Desense Capacitors



BOM_COST_GROUP=DISPLAY

SYNC_DATE=05/31/2019

PAGE TITLE: eDP Display Connector

Apple Inc.

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REVISION: 4.0.0
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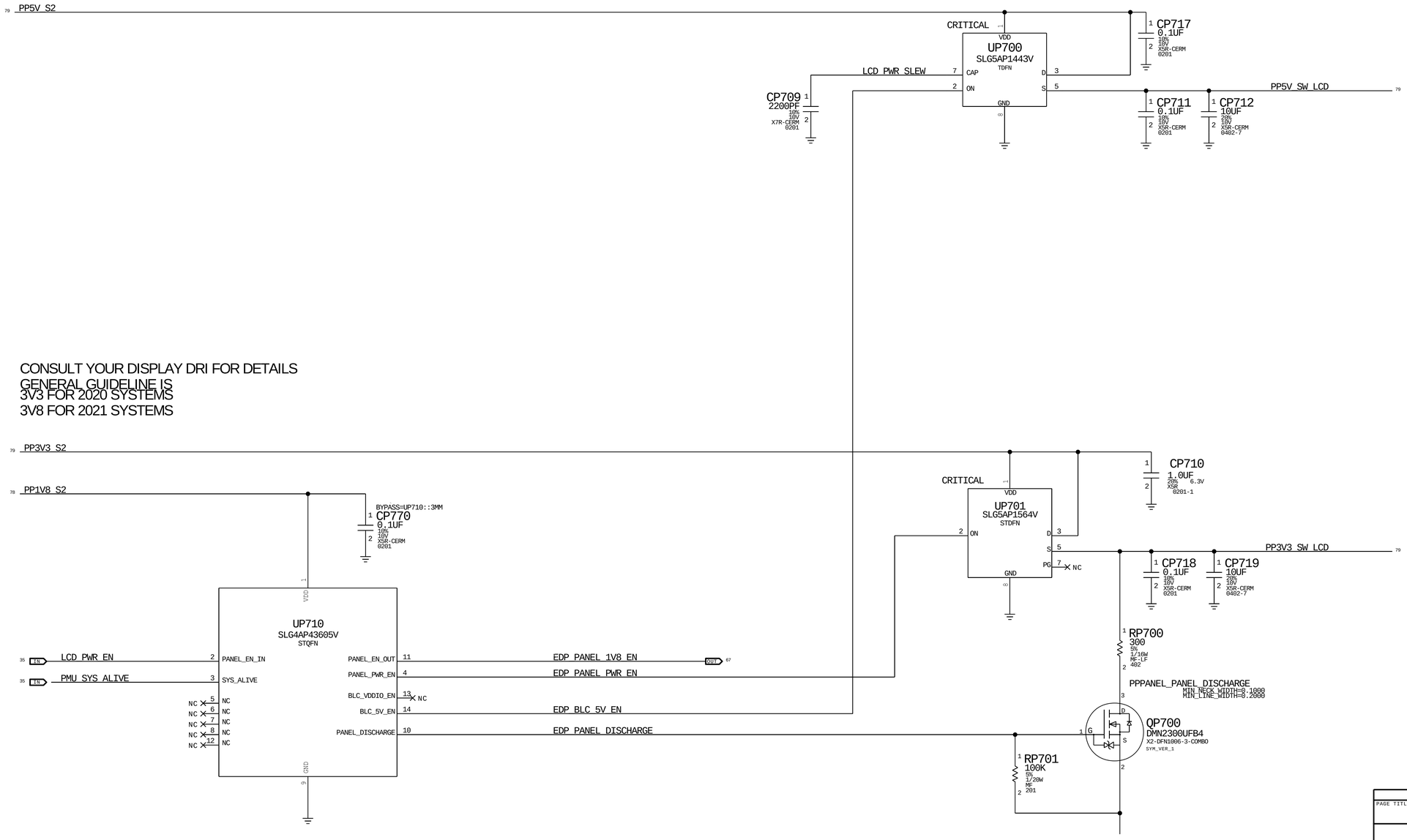
*** OK2INTEGRATE ***



SYNC_DATE=05/31/2019

PAGE TITLE

DISPLAY POWER SEQUENCER

Apple Inc.

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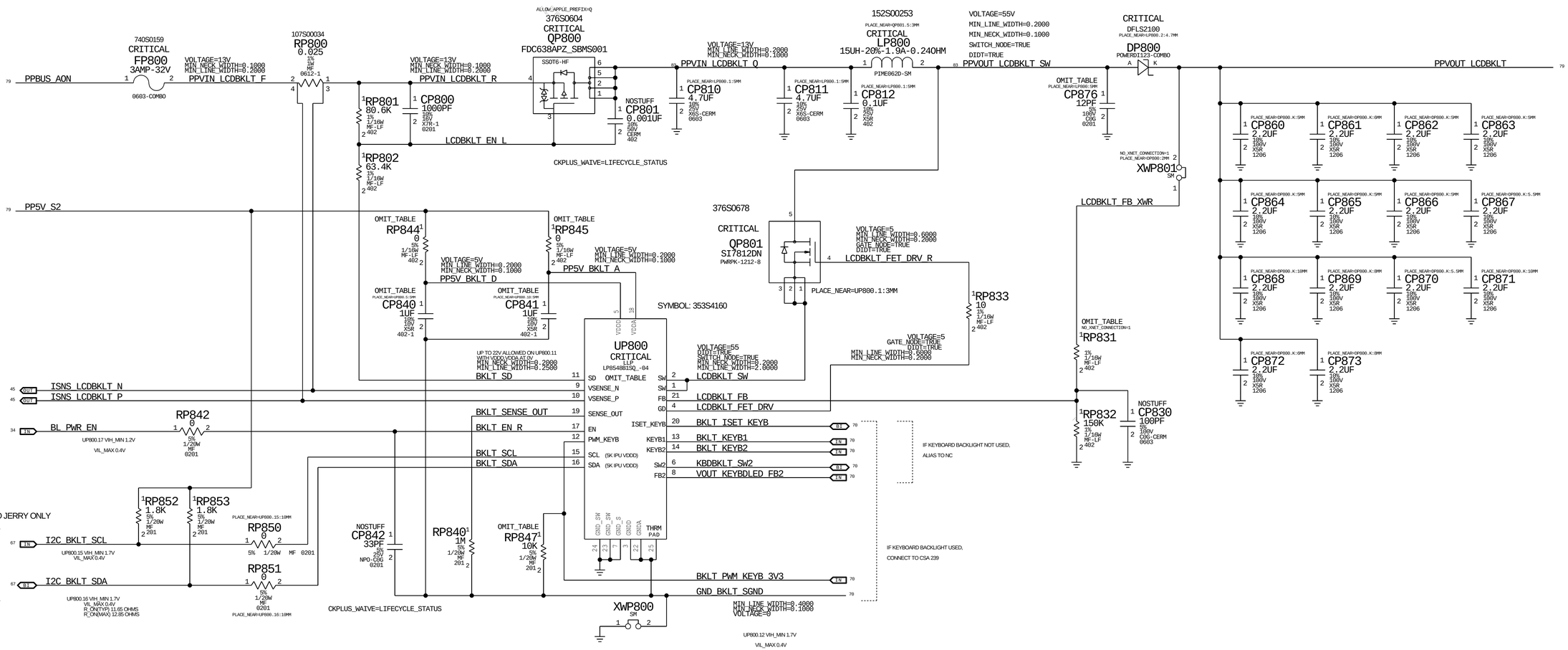
*** OK2INTEGRATE ***

BEN IC: DISPLAY/KBD BACKLIGHT BOOST CONVERTER

371S00077 (COMBO) FOOTPRINT IN LAYOUT



BEN IC VERSION TO MATCH VERSION OF JERRY IC IS ON THE PANEL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S4160	1	IC,LP8548B1-04,DC/DC CVTR,BOOST,QFN-24	UP800		BLC_BEN_IC:V4
353S02256	1	IC,LP8548B1A-07,DC/DC BOOST CVTR,QFN24	UP800		BLC_BEN_IC:V7

BACKLIGHT SWITCH NODE DESENSE OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00141	1	CAP,C0G,12PF,5%,100V,0201	CP876		BLC_SW_NODE_DESENSE

10K IF KEYBOARD PWM INPUT IS NOT PRESENT (J132, J213)
100K IF KEYBOARD PWM INPUT IS PRESENT (J152)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S0007	1	RES,MF,1/20W,10K OHM,5,0201,SMD	RP847		BLC_KBD_BOOST_USED:NO
118S0014	1	RES,MF,100KOHM,1,1/20W,0201	RP847		BLC_KBD_BOOST_USED:YES

BACKLIGHT BOOST VOLTAGE LEVEL BASED ON NUMBER OF LEDS PER STRING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0339	1	RES,MTL FILM,1/16W,18.2K,1,0402,SM,LF	RP831		BLC_LEDS_PER_STRING:16
114S0359	1	RES,MTL FILM,1/16W,28.7K,1,0402,SM,LF	RP831		BLC_LEDS_PER_STRING:18

BOM OPTION FOR BLC 5V RC FILTER, BASED ON PER PROJECT 5V RIPPLE CHARACTERIZATION.
AS COMPARED TO BLC TEAM'S 50 MV RIPPLE SPEC FOR VDDD & VDDA, SEE <RDAR://50882542>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	RP844,RP845		BLC_5V_SERIES:0_OHM
114S0023	2	RES,MTL FILM,1/16W,10 OHM,1,0402,SMD,LF	RP844,RP845		BLC_5V_SERIES:10_OHM
138S0614	2	CAP,CER,X5R,1UF,10%,10V,0402	CP840,CP841		BLC_5V_CAP:1_UF
138S00070	2	CAP,CER,X5R,4.7UF,20%,25V,0402	CP840,CP841		BLC_5V_CAP:4P7_UF

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=ref_blc_ben SYNC_DATE=05/31/2019

PAGE TITLE
BEN: CONTROLLER

Apple Inc.

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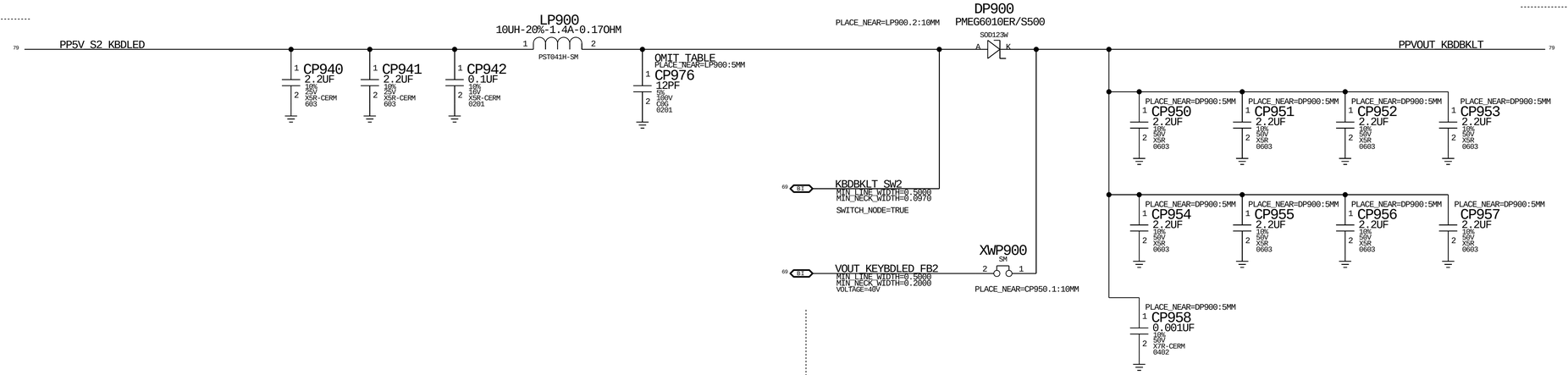
*** OK2INTEGRATE ***

BEN IC: KEYBOARD LED DRIVER

THIS PAGE IS ONLY TO BE INCLUDED IF THE KEYBOARD BACKLIGHT
IS CONTROLLED BY THE BEN ON PAGE 238

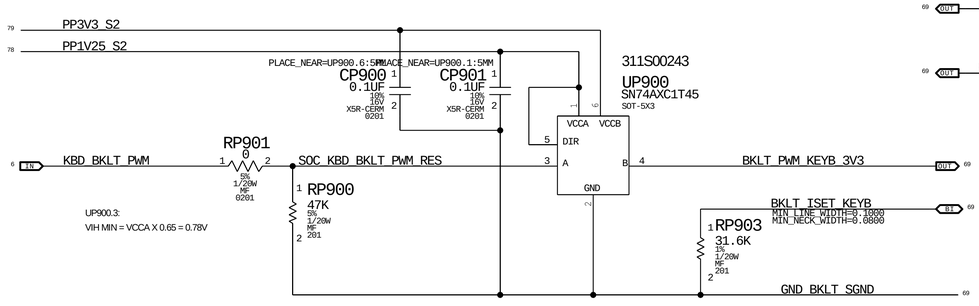
KEYBOARD BACKLIGHT
POWER & CONTROL
SIGNALS FROM
SYSTEM

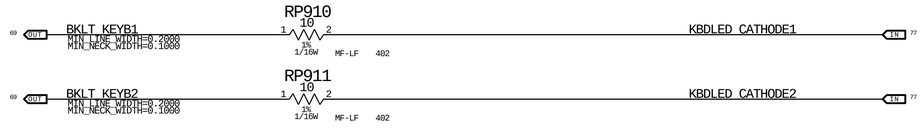


KEYBOARD BACKLIGHT
CONNECTOR SIGNALS

KEYBOARD BKLT PWM LEVEL-SHIFTER

UP900.4: VOH_MIN = 2.3V
VOL_MAX = 0.1V @ PWM_KEYB I_MAX OF 1UA





OFF-PAGE SIGNALS ON THIS VERTICAL LINE CONNECT TO BEN UP800

ON PAGE 238

KEYBOARD SWITCH NODE DESENSE OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00141	1	CAP,C0G,12PF,5%,100V,0201	CP976		BLC_KBD_SW_NODE_DESENSE

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=ref_blc_ben SYNC_DATE=11/20/2019

PAGE TITLE
BEN: KEYBOARD

Apple Inc.

DRAWING NUMBER	051-05392
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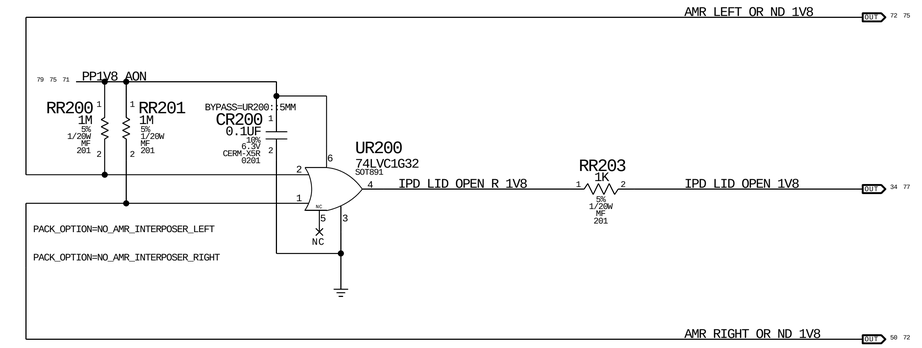
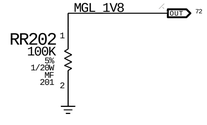
*** OK2INTEGRATE ***

Lid Detect Sensors

Clamshell Open = High
Clamshell Closed = Low





BOM_COST_GROUP=SYSTEM

SYNC_MASTER=ref_secdis_amr SYNC_DATE=05/31/2019

PAGE TITLE

SECDIS: AMR

Apple Inc.

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*** OK2INTEGRATE ***

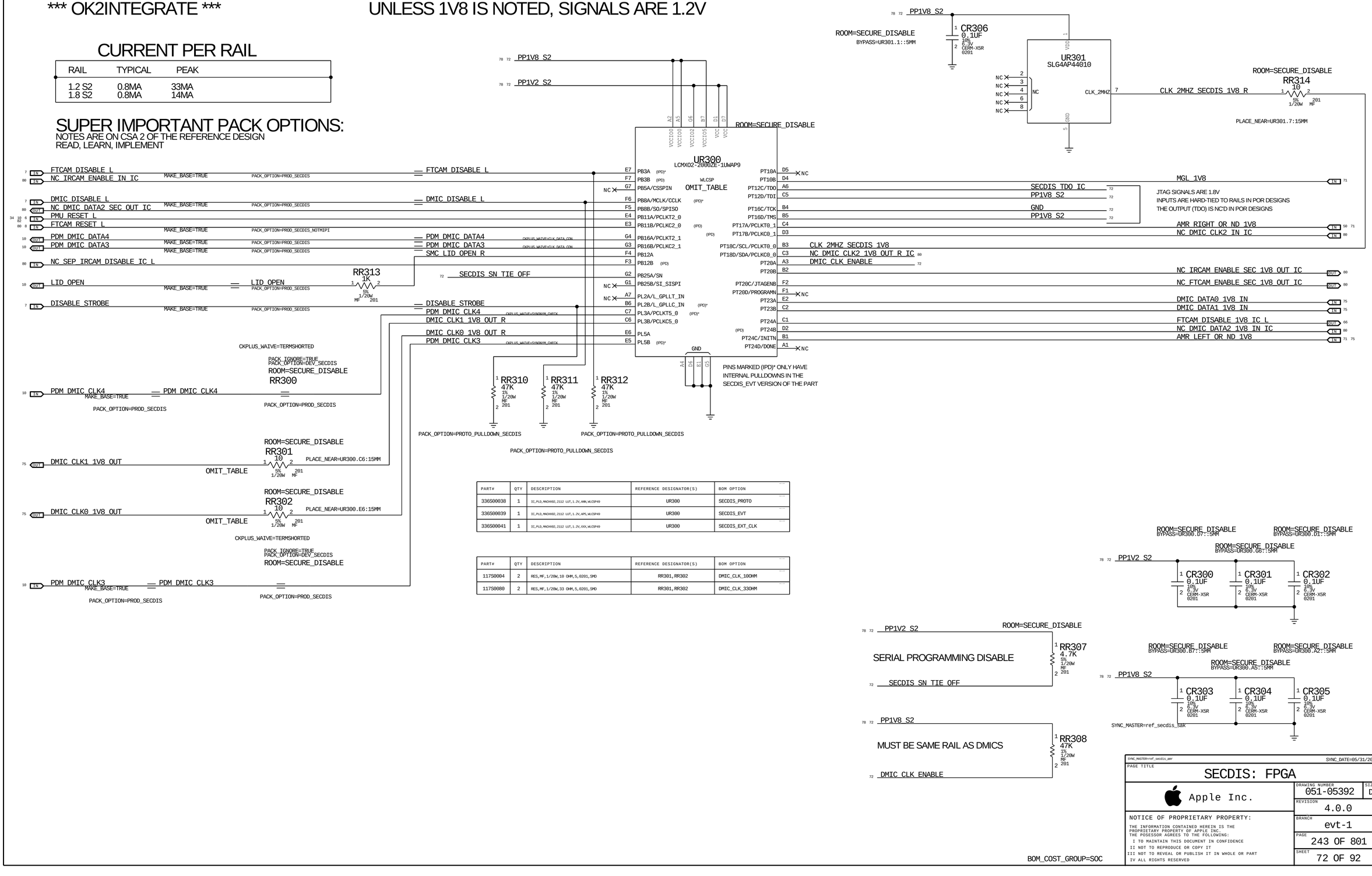
UNLESS 1V8 IS NOTED, SIGNALS ARE 1.2V

CURRENT PER RAIL

RAIL	TYPICAL	PEAK
1.2 S2	0.8MA	33MA
1.8 S2	0.8MA	14MA

SUPER IMPORTANT PACK OPTIONS:

NOTES ARE ON CSA 2 OF THE REFERENCE DESIGN
READ, LEARN, IMPLEMENT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
336S00038	1	IC,PLD,MACHXO2,2112 LUT,1.2V,ANN,WLCSP49	UR300	SECDIS_PROTO
336S00039	1	IC,PLD,MACHXO2,2112 LUT,1.2V,APS,WLCSP49	UR300	SECDIS_EVT
336S00041	1	IC,PLD,MACHXO2,2112 LUT,1.2V,XXX,WLCSP49	UR300	SECDIS_EXT_CLK

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0004	2	RES,MF,1/20W,10 OHM,5,0201,SMD	RR301,RR302	DMIC_CLK_10OHM
117S0080	2	RES,MF,1/20W,33 OHM,5,0201,SMD	RR301,RR302	DMIC_CLK_33OHM

SYNC_MASTER=ref_secdis_amr — SYNC_DATE=05/31/2019

PAGE TITLE: SECDIS: FPGA

Apple Inc.

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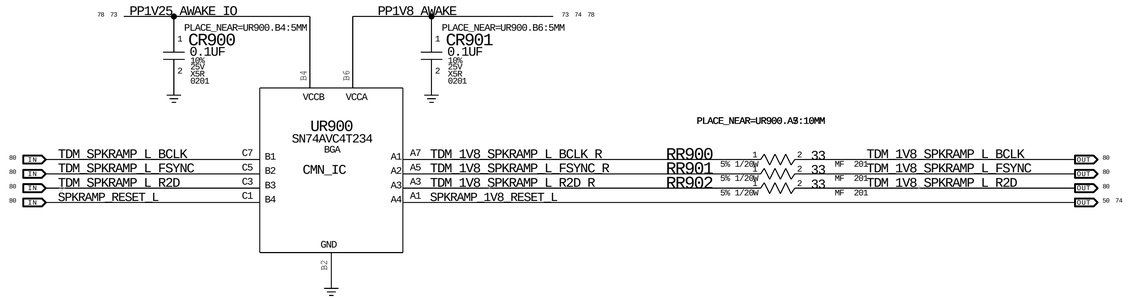
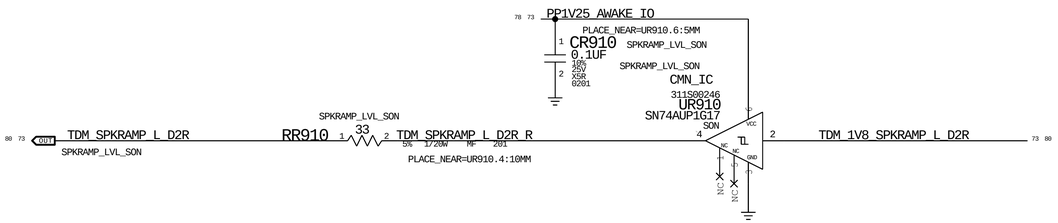
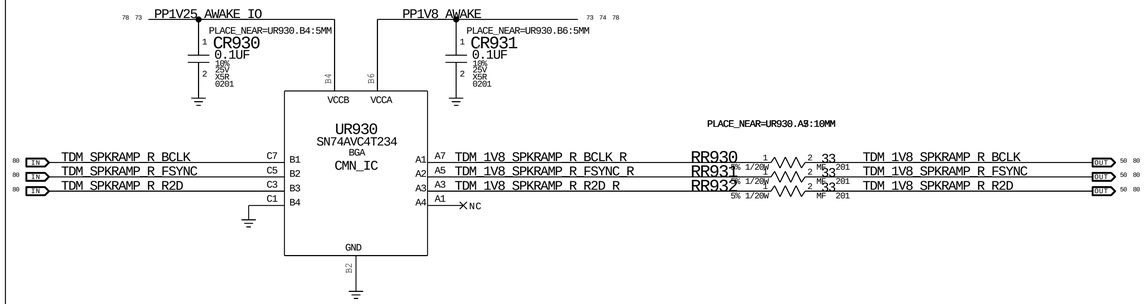
A Left Speaker Amplifier TDM Level Translator



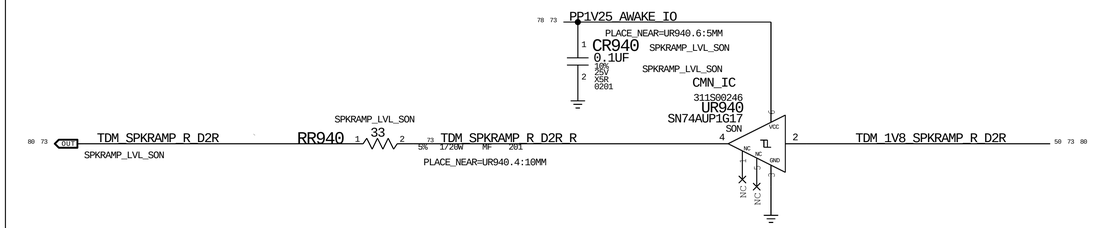
B Left Speaker Amplifier TDM Output Level Translator



C Right Speaker Amplifier TDM Level Translator



D Right Speaker Amplifier TDM Output Level Translator



BOM_COST_GROUP=AUDIO

SYNC_MASTER=ref_spkramp_tas5770 SYNC_DATE=05/31/2019

PAGE TITLE
Audio Level Shifters

Apple Inc.

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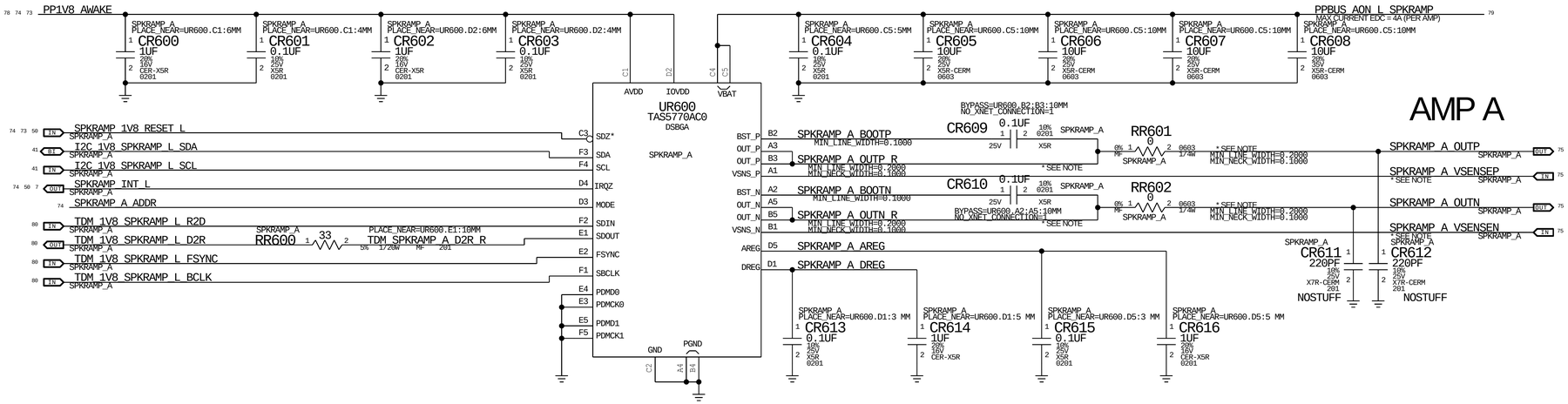
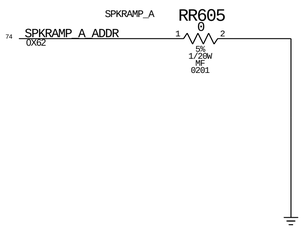
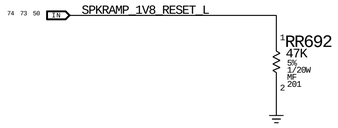
*** OK2INTEGRATE ***







NOTES:

- CHECK THAT SPKRAMP_INT_L HAS IPU ON SOC SIDE.
- VSENSEP/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
  - SPKRAMP_XX_OUTP/N_R
  - SPKRAMP_XX_OUTP/N
  - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.

BOM_COST_GROUP=AUDIO

SYNC_MASTER=ref_spkramp_tas5770 SYNC_DATE=05/31/2019

PAGE TITLE: AUDIO AMPLIFIERS (1/2)

Apple Inc.

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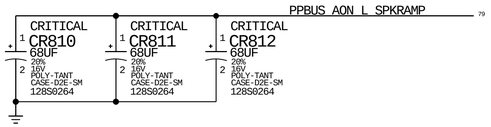
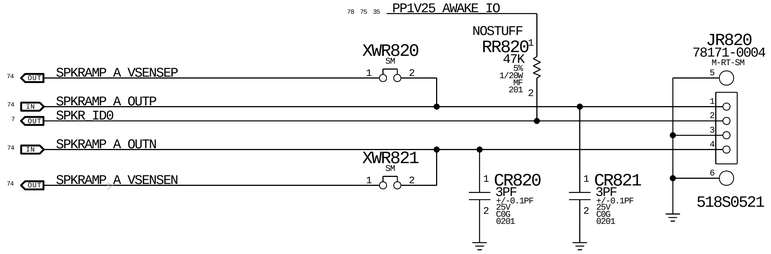
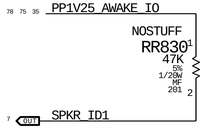
A Left Speaker Amplifier Bulk Capacitors



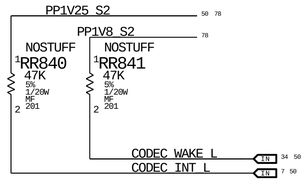
B Left Speaker Connector



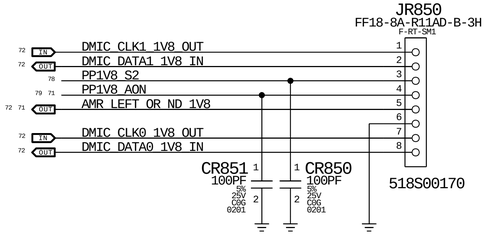
C Right Speaker ID



D Audio Jack CODEC Pull-Ups



E DMic Connector



BOM_COST_GROUP=AUDIO

SYNC_MASTER=tga_140 SYNC_DATE=05/31/2019

PAGE TITLE

Audio Connectors

Apple Inc.

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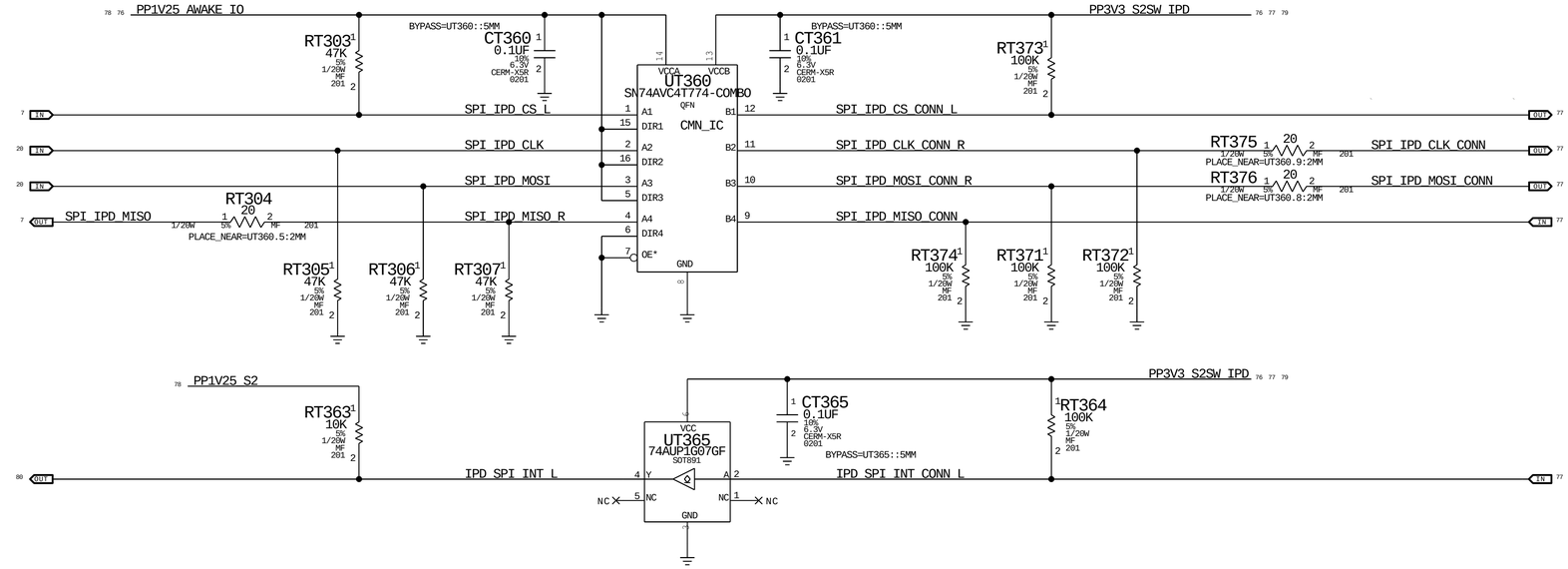
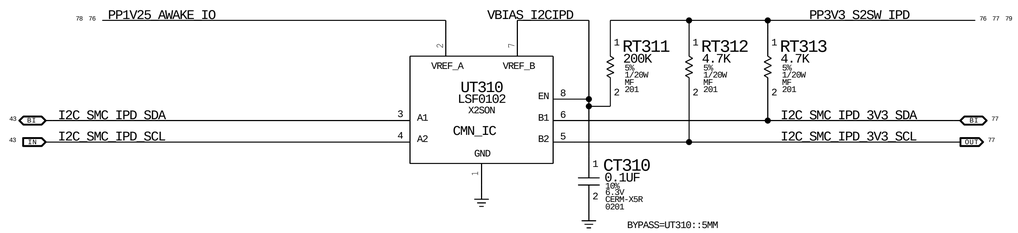
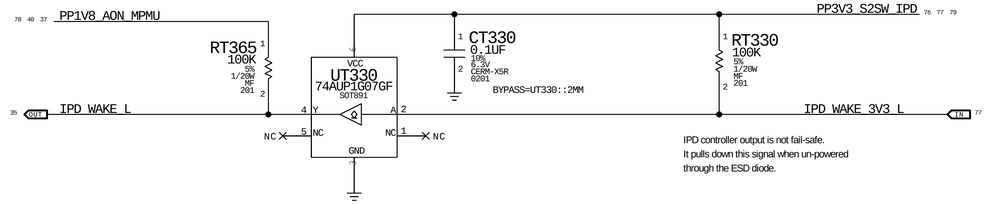
A Trackpad SPI Bus Level Shifter (+1.2V to +3.3V)



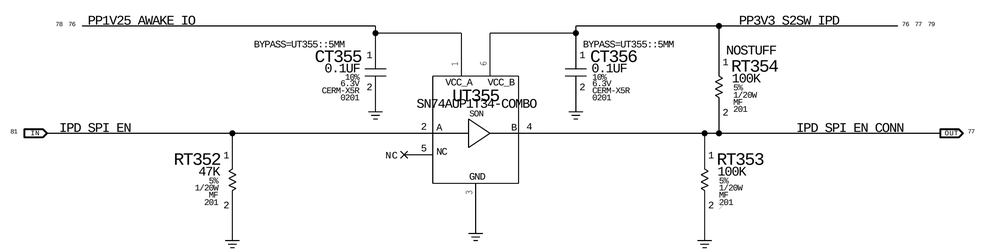
B Trackpad I2C Bus Level Shifter



C Trackpad Wake Level Shifter



D Trackpad SPI Enable Level Shifter



BOM_COST_GROUP=TRACKPAD

SYNC_DATE=05/31/2019

PAGE TITLE: Trackpad Support

Apple Inc.

DRAWING NUMBER: 051-05392 | SIZE: D

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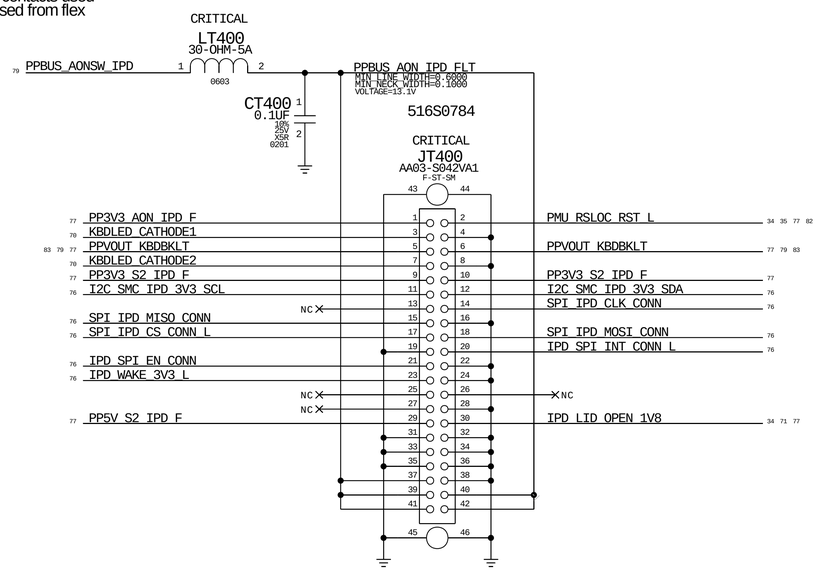
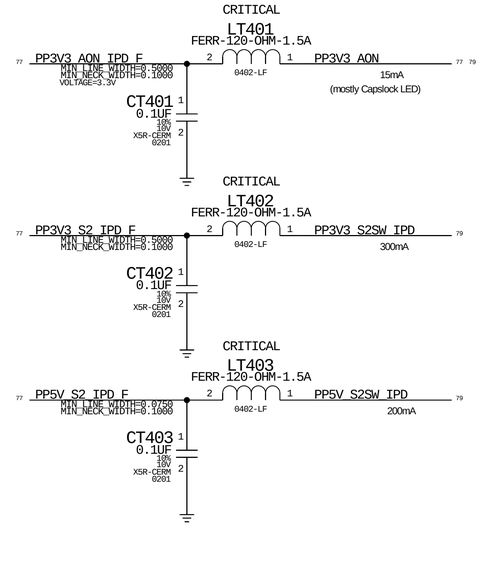
SHEET: 76 OF 92

A IPD B2B CONNECTOR

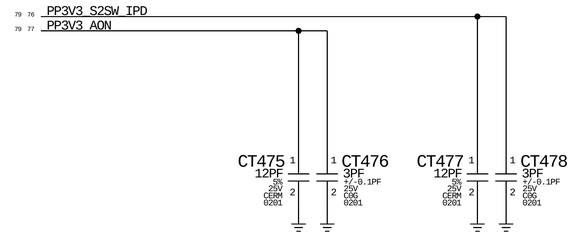
Bottom side contacts used
Pinout reversed from flex



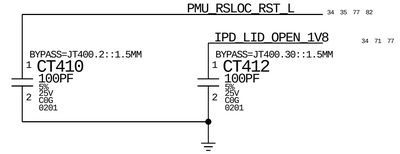
B IPD Power Filters



C IPD Desense



D IPD Control



F IPD Connector Bosses

860-01262

SHT400
BOSS-3.050D1.15ID-1.11H-SM

SHT401
BOSS-3.050D1.15ID-1.11H-SM

BOM_COST_GROUP=TRACKPAD

SYNC_DATE=05/31/2019

PAGE TITLE
IPD Combined Connector

Apple Inc.

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POWER CONNECTIONS

SERA BUCK0 (ACTIVE)

PPVDD_PCPU_AWAKE
MAKE_BASE=TRUE
VOLTAGE=1.06V
→ PPVDD_PCPU_AWAKE (32)
→ PPVDD_PCPU_AWAKE (13, 18)

SERA BUCK1 (SW CTRL)

83 PPVDD_GPU_AWAKE
MAKE_BASE=TRUE
VOLTAGE=1.06V
→ PPVDD_GPU_AWAKE (32)
→ PPVDD_GPU_AWAKE (13, 18)

SERA BUCK2 (SLEEP1)

83 PPVDD_SOC_S1
MAKE_BASE=TRUE
VOLTAGE=0.86V
→ PPVDD_SOC_S1 (32, 35)
→ PPVDD_SOC_S1 (13)

SERA BUCK3 (SLEEP3)

PP1V8_S2
MAKE_BASE=TRUE
VOLTAGE=1.8V
→ PP1V8_S2 (33)
→ PP1V8_S2 (54)
→ PP1V8_S2 (54)
72 PP1V8_S2 → PP1V8_S2 (29)
21 PP1V8_S2 → PP1V8_S2 (28)
54 PP1V8_S2 → PP1V8_S2 (32)
78 54 PP1V8_S2 → PP1V8_S2 (40)
78 75 PP1V8_S2 → PP1V8_S2 (33)
78 54 PP1V8_S2 → PP1V8_S2 (75, 78)
60 PP1V8_S2 → PP1V8_S2 (75)
PP1V8_S2 (23, 24)
49 PP1V8_S2
49 PP1V8_S2 → PP1V8_S2 (68)
→ PP1V8_S2 (42)
→ PP1V8_S2 (66)
→ PP1V8_S2 (42)
→ PP1V8_S2 (43)

SIMETRA BUCK4 (SLEEP3)

83 PP1V06_S2SW_DRAM
MAKE_BASE=TRUE
VOLTAGE=1.1V
→ PP1V06_S2SW_DRAM (28)
→ PP1V06_S2SW_DRAM (11, 18)
→ PP1V06_S2SW_DRAM (29)

SIMETRA BUCK5 (SLEEP1)

PP0V764_S1_SRAM
MAKE_BASE=TRUE
VOLTAGE=0.8V
→ PP0V764_S1_SRAM (28)
→ PP0V764_S1_SRAM (14, 18)

SIMETRA BUCK6 (ACTIVE)

83 31 PP2V5_AWAKE_NAND
MAKE_BASE=TRUE
VOLTAGE=2.63V
→ PP2V5_AWAKE_NAND (28)
→ PP2V5_AWAKE_NAND (62, 63, 64)

SERA BUCK7 (ACTIVE)

PPVDD_CPU_SRAM_AWAKE
MAKE_BASE=TRUE
VOLTAGE=1.1V
→ PPVDD_CPU_SRAM_AWAKE (33)
→ PPVDD_CPU_SRAM_AWAKE (14, 18)

SERA BUCK8 (SW CTRL)

83 PPVDD_DISP_S1
MAKE_BASE=TRUE
VOLTAGE=0.94V
→ PPVDD_DISP_S1 (33)
→ PPVDD_DISP_S1 (13, 18)

SERA BUCK9 (SLEEP1)

PPVDD_DCS_S1
MAKE_BASE=TRUE
VOLTAGE=0.85V
→ PPVDD_DCS_S1 (33)
→ PPVDD_DCS_S1 (14, 18)

SIMETRA BUCK10 (SLEEP1)

83 PP0V6_S1_VDDQL
MAKE_BASE=TRUE
VOLTAGE=0.6V
→ PP0V6_S1_VDDQL (28)
→ PP0V6_S1_VDDQL (11, 18)

SERA BUCK11 (ACTIVE)

83 PPVDD_ECPU_AWAKE
MAKE_BASE=TRUE
VOLTAGE=1.06V
→ PPVDD_ECPU_AWAKE (33)
→ PPVDD_ECPU_AWAKE (13, 18)

SIMETRA BUCK12 (ACTIVE)

PP0V88_S1
MAKE_BASE=TRUE
VOLTAGE=0.88V
→ PP0V88_S1 (28)
→ PP0V88_S1 (29)

SIMETRA BUCK13 (ACTIVE)

82 PP1V25_S2
MAKE_BASE=TRUE
VOLTAGE=1.25V
→ PP1V25_S2 (28)
→ PP1V25_S2 (10, 12)
42 PP1V25_S2 → PP1V25_S2 (12)
42 PP1V25_S2 → PP1V25_S2 (15)
76 PP1V25_S2 → PP1V25_S2 (15)
49 PP1V25_S2 → PP1V25_S2 (15)
43 PP1V25_S2 → PP1V25_S2 (21)
43 PP1V25_S2 → PP1V25_S2 (28)
43 PP1V25_S2 → PP1V25_S2 (29, 30)
43 PP1V25_S2 → PP1V25_S2 (33)
41 PP1V25_S2 → PP1V25_S2 (32)
PP1V25_S2 (53, 55, 56)
PP1V25_S2 (24)
75 56 PP1V25_S2 → PP1V25_S2 (70)
34 PP1V25_S2 → PP1V25_S2 (29)
66 PP1V25_S2 → PP1V25_S2 (35)
58 PP1V25_S2

SERA BUCK14 (ACTIVE)

PP1V4_LDO_PREREG
MAKE_BASE=TRUE
VOLTAGE=1.40V
→ PP1V4_LDO_PREREG (35)
→ PP1V4_LDO_PREREG (35)

SERA LDO1 (SLEEP2)

NC_MPMU_VLDO1
MAKE_BASE=TRUE
→ NC_MPMU_VLDO1 (34)

SERA LDO2 (SLEEP2)

SERA LDO3 (SLP_S2R)

PP1V2_S2
MAKE_BASE=TRUE
VOLTAGE=1.2V
→ PP1V2_S2 (34)
→ PP1V2_S2 (72)

SIMETRA LDO4 (SW CTRL)

83 PP0V72_S2_VDD_LOW
MAKE_BASE=TRUE
VOLTAGE=0.72V
→ PP0V72_S2_VDD_LOW (29)
→ PP0V72_S2_VDD_LOW (15, 18)
→ PP0V72_S2_VDD_LOW (15)
→ PP0V72_S2_VDD_LOW (15)
→ PP0V72_S2_VDD_LOW (15)
→ PP0V72_S2_VDD_LOW (15)

SERA LDO7 (SW CTRL)

PP3V3_S2_UPC
MAKE_BASE=TRUE
VOLTAGE=3.3V
→ PP3V3_S2_UPC (34)
→ PP3V3_S2_UPC (53, 55, 56)

SIMETRA LDO8 (SLEEP2)

83 PP1V2_AWAKE_PLL
MAKE_BASE=TRUE
VOLTAGE=1.2V
→ PP1V2_AWAKE_PLL (29)
→ PP1V2_AWAKE_PLL (15)
→ PP1V2_AWAKE_PLL (11)
→ PP1V2_AWAKE_PLL (15)
→ PP1V2_AWAKE_PLL (15)

SERA LDO9 (ACTIVE)

PP1V8_AON_MPMU
MAKE_BASE=TRUE
→ PP1V8_AON_MPMU (34)
→ PP1V8_AON_MPMU (30, 34)
→ PP1V8_AON_MPMU (24)
→ PP1V8_AON_MPMU (36)
→ PP1V8_AON_MPMU (37, 40, 76)

SERA LDO10 (ACTIVE)

SIMETRA LDO11 (SLEEP2)

PP0V855_S2SW_CIO
MAKE_BASE=TRUE
VOLTAGE=0.86V
→ PP0V855_S2SW_CIO (29)
→ PP0V855_S2SW_CIO (15)
→ PP0V855_S2SW_CIO (15)

SIMETRA LDO12 (SLEEP2)

83 PP0V805_S1_VDD_FIXED
MAKE_BASE=TRUE
VOLTAGE=0.805V
→ PP0V805_S1_VDD_FIXED (29)
→ PP0V805_S1_VDD_FIXED (15, 18)
→ PP0V805_S1_VDD_FIXED (15)
→ PP0V805_S1_VDD_FIXED (15)
→ PP0V805_S1_VDD_FIXED (15)
→ PP0V805_S1_VDD_FIXED (15, 18)
→ PP0V805_S1_VDD_FIXED (15)
→ PP0V805_S1_VDD_FIXED (15)
→ PP0V805_S1_VDD_FIXED (15)
→ PP0V805_S1_VDD_FIXED (15)

SERA LDO13 (SW CTRL)

SERA LDO16 (SW CTRL)

SERA LDO19 (SPARE)

SIMETRA LDO20 (SW CTRL)

83 PP1V2_S2_CIO
MAKE_BASE=TRUE
→ PP1V2_S2_CIO (29)
→ PP1V2_S2_CIO (15)
→ PP1V2_S2_CIO (15)

SERA SW1 (ACTIVE)

PP1V8_AWAKE
MAKE_BASE=TRUE
→ PP1V8_AWAKE (33)
→ PP1V8_AWAKE (12)
→ PP1V8_AWAKE (73, 74)
→ PP1V8_AWAKE (5)
→ PP1V8_AWAKE (19)
→ PP1V8_AWAKE (19)
→ PP1V8_AWAKE (50)
→ PP1V8_AWAKE (41)

SERA SW3 (ACTIVE)

83 PP1V25_AWAKE_IO
MAKE_BASE=TRUE
→ PP1V25_AWAKE_IO (33)
→ PP1V25_AWAKE_IO (15)
→ PP1V25_AWAKE_IO (5, 6, 7, 9, 12)
→ PP1V25_AWAKE_IO (15)
→ PP1V25_AWAKE_IO (15)
→ PP1V25_AWAKE_IO (15)
→ PP1V25_AWAKE_IO (74)
→ PP1V25_AWAKE_IO (15)
→ PP1V25_AWAKE_IO (15)
→ PP1V25_AWAKE_IO (35, 75)
→ PP1V25_AWAKE_IO (76)
→ PP1V25_AWAKE_IO (73)
→ PP1V25_AWAKE_IO (50)
→ PP1V25_AWAKE_IO (5)
→ PP1V25_AWAKE_IO (19)
→ PP1V25_AWAKE_IO (41)
→ PP1V25_AWAKE_IO (41)
→ PP1V25_AWAKE_IO (41)

SIMETRA SW4 (SLEEP2)

SIMETRA SW5 (SLEEP2)

83 PP1V25_AWAKE_NAND
MAKE_BASE=TRUE
VOLTAGE=1.25V
→ PP1V25_AWAKE_NAND (29)
→ PP1V25_AWAKE_NAND (62, 63)

SIMETRA SW6 (SLEEP2) PARALLEL
SIMETRA SW7 (SLEEP2) PARALLEL

83 PP0V88_AWAKE_NAND
MAKE_BASE=TRUE
VOLTAGE=0.88V
→ PP0V88_AWAKE_NAND (29)
→ PP0V88_AWAKE_NAND (62)
→ PP0V88_AWAKE_NAND (63)

SYNC_DATE=05/31/2019

PAGE TITLE
Power Aliases - 1

Apple Inc.

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PBUS Rails

U7000 - PBUS

23 PPBUS_AON
- PPBUS_AON (83)
  - MIN_LINE_WIDTH=0.0970
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=13.1V
  - MAKE_BASE=TRUE
- PPBUS_AON (27)
- PPBUS_AON (69)
- PPBUS_AON (46)
- PPBUS_AON (50)
- PPBUS_AON (40)
- PPBUS_AON (44)
- PPBUS_AON (25 26)
- PPBUS_AON (32)
- PPBUS_AON (44)
- PPBUS_AON (44)

44 PPBUS_5VS2_VIN
- PPBUS_5VS2_VIN
  - MIN_LINE_WIDTH=0.0970
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=13.1V
  - MAKE_BASE=TRUE
- PPBUS_5VS2_VIN (38)

44 PPBUS_3V3S2_VIN
- PPBUS_3V3S2_VIN
  - MIN_LINE_WIDTH=0.0970
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=13.1V
  - MAKE_BASE=TRUE
- PPBUS_3V3S2_VIN (39)

46 PPBUS_AON_L_SPKRAMP
- PPBUS_AON_L_SPKRAMP (83)
  - MIN_LINE_WIDTH=0.0970
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=13.1V
  - MAKE_BASE=TRUE
- PPBUS_AON_L_SPKRAMP (75)
- PPBUS_AON_L_SPKRAMP (74)

40 PPBUS_AONSW_IPD
- PPBUS_AONSW_IPD (83)
  - MIN_LINE_WIDTH=0.0970
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=13.1V
  - MAKE_BASE=TRUE
- PPBUS_AONSW_IPD (77)

53 PPDCIN_AONSW
- PPDCIN_AONSW (83)
  - MIN_LINE_WIDTH=0.0970
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=20V
  - MAKE_BASE=TRUE
- PPDCIN_AONSW (23)
- PPDCIN_AONSW (44)

U7550 - 5V G3S

38 PP5V_S2 (Sourced from PBus, Enabled by P5VG3S_EN)
- PP5V_S2 (83)
  - MIN_LINE_WIDTH=0.2000
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=5V
  - MAKE_BASE=TRUE
- PP5V_S2 (37)
- PP5V_S2 (46)
- PP5V_S2 (67)
- PP5V_S2 (69)
- PP5V_S2 (38)
- PP5V_S2 (68)
- PP5V_S2 (55 56)
- PP5V_S2 (55 56)
- PP5V_S2 (40)
- PP5V_S2 (27)

46 PP5V_S2_KBDLED
- PP5V_S2_KBDLED (83)
  - MIN_LINE_WIDTH=0.0970
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=5V
  - MAKE_BASE=TRUE
- PP5V_S2_KBDLED (70)

25 PP5V_AON_P3V8VRLDO
- PP5V_AON_P3V8VRLDO
  - MIN_LINE_WIDTH=0.0000
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=5V
  - MAKE_BASE=TRUE
- PP5V_AON_P3V8VRLDO (25)

68 PP5V_SW_LCD
- PP5V_SW_LCD (67)
  - MIN_LINE_WIDTH=0.2000
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=5V
  - MAKE_BASE=TRUE

40 PP5V_S2SW_IPD
- PP5V_S2SW_IPD (83)
  - MIN_LINE_WIDTH=0.2000
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=5V
  - MAKE_BASE=TRUE
- PP5V_S2SW_IPD (77)
- PP5V_S2SW_IPD (46)

3V3 Rails

UXXXX - 3V3_S2

39 PP3V3_S2 (Sourced from PBus, Enabled by ????)
- PP3V3_S2 (82)
  - MIN_LINE_WIDTH=0.1000
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=3.3V
  - MAKE_BASE=TRUE
- PP3V3_S2 (46)
- PP3V3_S2 (37)
- PP3V3_S2 (66)
- PP3V3_S2 (70)
- PP3V3_S2 (40)
- PP3V3_S2 (68)
- PP3V3_S2 (40)
- PP3V3_S2 (39)
- PP3V3_S2 (43)

46 PP3V3_S2_WLBT
- PP3V3_S2_WLBT (83)
  - MIN_LINE_WIDTH=0.0970
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=3.3V
  - MAKE_BASE=TRUE
- PP3V3_S2_WLBT (60)

40 PP3V3_S2SW_SNS
- PP3V3_S2SW_SNS (83)
  - MIN_LINE_WIDTH=0.0970
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=3.3V
  - MAKE_BASE=TRUE
- PP3V3_S2SW_SNS (44 45 46)

40 PP3V3_S2SW_IPD
- PP3V3_S2SW_IPD (83)
  - MIN_LINE_WIDTH=0.0970
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=3.3V
  - MAKE_BASE=TRUE
- PP3V3_S2SW_IPD (76 77)
- PP3V3_S2SW_IPD (77)

68 PP3V3_SW_LCD
- PP3V3_SW_LCD (67)
  - MIN_LINE_WIDTH=0.2000
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=3.3V
  - MAKE_BASE=TRUE
- PP3V3_SW_LCD (41)

36 PP3V3_AON (Sourced from PBus)
- PP3V3_AON (82)
  - MIN_LINE_WIDTH=0.1000
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=3.3V
  - MAKE_BASE=TRUE
- PP3V3_AON (77)
- PP3V3_AON (43)
- PP3V3_AON (35)

PP1V8_AON
- MAKE_BASE=TRUE
- VOLTAGE=1.8V
- PP1V8_AON (36)
- PP1V8_AON (50)
- PP1V8_AON (40)
- PP1V8_AON (35)
- PP1V8_AON (71 75)

PP1V8_S2SW_VDD1
- MAKE_BASE=TRUE
- VOLTAGE=1.8V
- PP1V8_S2SW_VDD1 (40)
- PP1V8_S2SW_VDD1 (11 18)

NEED TO CHECK THE SPLIT
TO DIFFERENT SWITCH OUTPUTS.

PPVOUT_LCDBKLT
- MIN_LINE_WIDTH=0.5000
- MIN_NECK_WIDTH=0.1000
- VOLTAGE=35V
- MAKE_BASE=TRUE
- PPVOUT_LCDBKLT (67 83)
- PPVOUT_LCDBKLT (69)

PPVOUT_KBDBKLT
- MIN_LINE_WIDTH=0.1000
- MIN_NECK_WIDTH=0.1000
- VOLTAGE=40V
- MAKE_BASE=TRUE
- PPVOUT_KBDBKLT (77 83)
- PPVOUT_KBDBKLT (70)

PP3V3_S2SW_USBC0
- MAKE_BASE=TRUE
- PP3V3_S2SW_USBC0 (51)
- PP3V3_S2SW_USBC0 (51 53)
- PP3V3_S2SW_USBC0 (51 53)
- PP3V3_S2SW_USBC0 (58)
- PP3V3_S2SW_USBC0 (58)

PP3V3_S2SW_USBC1
- MAKE_BASE=TRUE
- PP3V3_S2SW_USBC1 (52)
- PP3V3_S2SW_USBC1 (52 53)
- PP3V3_S2SW_USBC1 (52 53)
- PP3V3_S2SW_USBC1 (58)
- PP3V3_S2SW_USBC1 (58)

CHARGER MAIN

83 82 PP3V8_AON_VDDMAIN
- MAKE_BASE=TRUE
- VOLTAGE=3.8V
- PP3V8_AON_VDDMAIN (26)
- PP3V8_AON_VDDMAIN (32 34 35)
- PP3V8_AON_VDDMAIN (28 29)
- PP3V8_AON_VDDMAIN (58)
- PP3V8_AON_VDDMAIN (40)
- PP3V8_AON_VDDMAIN (36)
- PP3V8_AON_VDDMAIN (36)
- PP3V8_AON_VDDMAIN (27)
- PP3V8_AON_VDDMAIN (21)
- PP3V8_AON_VDDMAIN (51)
- PP3V8_AON_VDDMAIN (52)
- PP3V8_AON_VDDMAIN (22)
- PP3V8_AON_VDDMAIN (32)
- PP3V8_AON_VDDMAIN (37)

Digital Ground

GND
- VOLTAGE=0V
- MIN_LINE_WIDTH=0.1000
- MIN_NECK_WIDTH=0.0800

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NC_DFR_1V8_DISP_INT	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_1V8_DISP_INT				
NC_DFR_1V8_DISP_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_1V8_DISP_RESET_L				
NC_DFR_1V8_TOUCH_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_1V8_TOUCH_RESET_L				
NC_DFR_DISP_TE	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_DISP_TE				
NC_DFR_PWR_EN	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_PWR_EN				
NC_HDMI_CEC_AOP_RX	MAKE_BASE=TRUE	NO_TEST=1	NC_HDMI_CEC_AOP_RX				
NC_HDMI_CEC_AOP_TX	MAKE_BASE=TRUE	NO_TEST=1	NC_HDMI_CEC_AOP_TX				
NC_HDMI_HPD_AOP	MAKE_BASE=TRUE	NO_TEST=1	NC_HDMI_HPD_AOP				
NC_MIPI_DFR_CLKN	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI_DFR_CLKN				
NC_MIPI_DFR_CLKP	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI_DFR_CLKP				
NC_MIPI_DFR_DATAN	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI_DFR_DATAN				
NC_MIPI_DFR_DATAP	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI_DFR_DATAP				
NC_PCIE_CLK100M_ENETN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_ENETN				
NC_PCIE_CLK100M_ENETP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_ENETP				
NC_PCIE_CLK100M_USBHCN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_USBHCN				
NC_PCIE_CLK100M_USBHCP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_USBHCP				
NC_PCIE_ENET_D2RN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_D2RN				
NC_PCIE_ENET_D2RP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_D2RP				
NC_PCIE_ENET_R2DCN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_R2DCN				
NC_PCIE_ENET_R2DCP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_R2DCP				
NC_PCIE_USBHC_D2RN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_USBHC_D2RN				
NC_PCIE_USBHC_D2RP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_USBHC_D2RP				
NC_PCIE_USBHC_R2DCN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_USBHC_R2DCN				
NC_PCIE_USBHC_R2DCP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_USBHC_R2DCP				
NC_SMC_FAN_PWM_SMC_SIL_LED_PWM	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_FAN_PWM_SMC_SIL_LED_PWM				
NC_SMC_FAN_TACH	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_FAN_TACH				
NC_SPI_DISP_BKLT_MOSI	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_DISP_BKLT_MOSI				
NC_SPI_DISP_BKLT_MISO	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_DISP_BKLT_MISO				
NC_SPI_DP2HDMI_HOLD_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_DP2HDMI_HOLD_L				
NC_NUB_SWD_TMS1	MAKE_BASE=TRUE	NO_TEST=1	NC_NUB_SWD_TMS1				
NC_I2C_SE_SCL	MAKE_BASE=TRUE	NO_TEST=1	NC_I2C_SE_SCL				
NC_I2C_SE_SDA	MAKE_BASE=TRUE	NO_TEST=1	NC_I2C_SE_SDA				
NC_DFR_TOUCH_INT_L	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_TOUCH_INT_L				
NC_UART_TCON_R2D	MAKE_BASE=TRUE	NO_TEST=1	NC_UART_TCON_R2D				
NC_ACDC_BURST_EN_L	MAKE_BASE=TRUE	NO_TEST=1	NC_ACDC_BURST_EN_L				
NC_ACDC_ID	MAKE_BASE=TRUE	NO_TEST=1	NC_ACDC_ID				
NC_CCG_SMC_I2C_INT_L	MAKE_BASE=TRUE	NO_TEST=1	NC_CCG_SMC_I2C_INT_L				
NC_BKLT_FAULT_INT_L	MAKE_BASE=TRUE	NO_TEST=1	NC_BKLT_FAULT_INT_L				
NC_DISP_BKLT_LSYNC	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_BKLT_LSYNC				
NC_ENET_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=1	NC_ENET_CLKREQ_L				
NC_ENET_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_ENET_RESET_L				
NC_USBHC_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_USBHC_RESET_L				
NC_DFR_TOUCH_CLK32K_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_TOUCH_CLK32K_RESET_L				
NC_AOP_FUNC0	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC0				
NC_AOP_FUNC3	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC3				
NC_AOP_FUNC2	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC2				
NC_SPI_R1_CS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_R1_CS_L				
NC_BKLT_PWR_ON	MAKE_BASE=TRUE	NO_TEST=1	NC_BKLT_PWR_ON				
NC_RF_BT_DED	MAKE_BASE=TRUE	NO_TEST=1	NC_RF_BT_DED				
NC_MIPI_FTCAM_DATA1P	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI_FTCAM_DATA1P				
NC_MIPI_FTCAM_DATA1N	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI_FTCAM_DATA1N				
NC_DMIC_CLK2_1V8_OUT_R_IC	MAKE_BASE=TRUE	NO_TEST=1	NC_DMIC_CLK2_1V8_OUT_R_IC				
NC_DMIC_CLK2_IN_IC	MAKE_BASE=TRUE	NO_TEST=1	NC_DMIC_CLK2_IN_IC				
NC_DMIC_DATA2_1V8_IN_IC	MAKE_BASE=TRUE	NO_TEST=1	NC_DMIC_DATA2_1V8_IN_IC				
NC_DMIC_DATA2_SEC_OUT_IC	MAKE_BASE=TRUE	NO_TEST=1	NC_DMIC_DATA2_SEC_OUT_IC				
NC_FTCAM_ENABLE_SEC_1V8_OUT_IC	MAKE_BASE=TRUE	NO_TEST=1	NC_FTCAM_ENABLE_SEC_1V8_OUT_IC				
NC_IRCAM_ENABLE_IN_IC	MAKE_BASE=TRUE	NO_TEST=1	NC_IRCAM_ENABLE_IN_IC				
NC_IRCAM_ENABLE_SEC_1V8_OUT_IC	MAKE_BASE=TRUE	NO_TEST=1	NC_IRCAM_ENABLE_SEC_1V8_OUT_IC				
FTCAM_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	FTCAM_RESET_L				
NC_SEP_IRCAM_DISABLE_IC_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SEP_IRCAM_DISABLE_IC_L				
NC_FTCAM_ENABLE_IN	MAKE_BASE=TRUE	NO_TEST=1	NC_FTCAM_ENABLE_IN				
NC_ENET_SYNC_1588	MAKE_BASE=TRUE	NO_TEST=1	NC_ENET_SYNC_1588				
NC_SPI_DFR_CS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_DFR_CS_L				
NC_SWD_UPC_SWDIO1	MAKE_BASE=TRUE	NO_TEST=1	NC_SWD_UPC_SWDIO1				
NC_ALS_INT_L	MAKE_BASE=TRUE	NO_TEST=1	NC_ALS_INT_L				
NC_SOC_TRIGGER2	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_TRIGGER2				
NC_BT_GPIO_4	MAKE_BASE=TRUE	NO_TEST=1	NC_BT_GPIO_4				
NC_SPMI_WLBT_CLK_1V8	MAKE_BASE=TRUE	NO_TEST=1	NC_SPMI_WLBT_CLK_1V8				
NC_SPMI_WLBT_DAT_1V8	MAKE_BASE=TRUE	NO_TEST=1	NC_SPMI_WLBT_DAT_1V8				
TOUCHID_PWR_EN	MAKE_BASE=TRUE		TOUCHID_PWR_EN				

USB2_ATC0_LS_P	MAKE_BASE=TRUE	USB2_ATC0_LS_P	
USB2_ATC0_LS_N	MAKE_BASE=TRUE	USB2_ATC0_LS_N	
USB2_ATC1_LS_P	MAKE_BASE=TRUE	USB2_ATC1_LS_P	
USB2_ATC1_LS_N	MAKE_BASE=TRUE	USB2_ATC1_LS_N	
USB_DBG_LS_P	MAKE_BASE=TRUE	USB_DBG_LS_P	
USB_DBG_LS_N	MAKE_BASE=TRUE	USB_DBG_LS_N	
CHGR_INT_L	MAKE_BASE=TRUE	CHGR_INT_L	
USBC_ATC0_R2D_P<1>	MAKE_BASE=TRUE	USBC_ATC0_R2D_P<1>	
USBC_ATC0_R2D_N<1>	MAKE_BASE=TRUE	USBC_ATC0_R2D_N<1>	
USBC0_D2R_P<1>	MAKE_BASE=TRUE	USBC0_D2R_P<1>	
USBC0_D2R_N<1>	MAKE_BASE=TRUE	USBC0_D2R_N<1>	
USBC_ATC0_R2D_P<2>	MAKE_BASE=TRUE	USBC_ATC0_R2D_P<2>	
USBC_ATC0_R2D_N<2>	MAKE_BASE=TRUE	USBC_ATC0_R2D_N<2>	
USBC0_D2R_P<2>	MAKE_BASE=TRUE	USBC0_D2R_P<2>	
USBC0_D2R_N<2>	MAKE_BASE=TRUE	USBC0_D2R_N<2>	
USBC_ATC0_D2R_C_P<1>	MAKE_BASE=TRUE	USBC_ATC0_D2R_C_P<1>	
USBC_ATC0_D2R_C_N<1>	MAKE_BASE=TRUE	USBC_ATC0_D2R_C_N<1>	
USBC0_R2D_CR_P<1>	MAKE_BASE=TRUE	USBC0_R2D_CR_P<1>	
USBC0_R2D_CR_N<1>	MAKE_BASE=TRUE	USBC0_R2D_CR_N<1>	
USBC_ATC0_D2R_C_P<2>	MAKE_BASE=TRUE	USBC_ATC0_D2R_C_P<2>	
USBC_ATC0_D2R_C_N<2>	MAKE_BASE=TRUE	USBC_ATC0_D2R_C_N<2>	
USBC0_R2D_CR_P<2>	MAKE_BASE=TRUE	USBC0_R2D_CR_P<2>	
USBC0_R2D_CR_N<2>	MAKE_BASE=TRUE	USBC0_R2D_CR_N<2>	
USBC_ATC1_R2D_P<1>	MAKE_BASE=TRUE	USBC_ATC1_R2D_P<1>	
USBC_ATC1_R2D_N<1>	MAKE_BASE=TRUE	USBC_ATC1_R2D_N<1>	
USBC1_D2R_P<1>	MAKE_BASE=TRUE	USBC1_D2R_P<1>	
USBC1_D2R_N<1>	MAKE_BASE=TRUE	USBC1_D2R_N<1>	
USBC_ATC1_R2D_P<2>	MAKE_BASE=TRUE	USBC_ATC1_R2D_P<2>	
USBC_ATC1_R2D_N<2>	MAKE_BASE=TRUE	USBC_ATC1_R2D_N<2>	
USBC1_D2R_P<2>	MAKE_BASE=TRUE	USBC1_D2R_P<2>	
USBC1_D2R_N<2>	MAKE_BASE=TRUE	USBC1_D2R_N<2>	
USBC_ATC1_D2R_C_P<1>	MAKE_BASE=TRUE	USBC_ATC1_D2R_C_P<1>	
USBC_ATC1_D2R_C_N<1>	MAKE_BASE=TRUE	USBC_ATC1_D2R_C_N<1>	
USBC1_R2D_CR_P<1>	MAKE_BASE=TRUE	USBC1_R2D_CR_P<1>	
USBC1_R2D_CR_N<1>	MAKE_BASE=TRUE	USBC1_R2D_CR_N<1>	
USBC_ATC1_D2R_C_P<2>	MAKE_BASE=TRUE	USBC_ATC1_D2R_C_P<2>	
USBC_ATC1_D2R_C_N<2>	MAKE_BASE=TRUE	USBC_ATC1_D2R_C_N<2>	
USBC1_R2D_CR_P<2>	MAKE_BASE=TRUE	USBC1_R2D_CR_P<2>	
USBC1_R2D_CR_N<2>	MAKE_BASE=TRUE	USBC1_R2D_CR_N<2>	
UART_TCON_D2R	MAKE_BASE=TRUE	UART_TCON_D2R	
IPD_SPI_INT_L	MAKE_BASE=TRUE	IPD_SPI_INT_L	
SOC_DOCK_CONNECT	MAKE_BASE=TRUE	SOC_DOCK_CONNECT	
SPKRAMP_RESET_L	MAKE_BASE=TRUE	SPKRAMP_RESET_L	
TDM_SPKRAMP_L_BCLK	MAKE_BASE=TRUE	TDM_SPKRAMP_L_BCLK	
TDM_SPKRAMP_L_FSYNC	MAKE_BASE=TRUE	TDM_SPKRAMP_L_FSYNC	
TDM_SPKRAMP_L_R2D	MAKE_BASE=TRUE	TDM_SPKRAMP_L_R2D	
TDM_SPKRAMP_L_D2R	MAKE_BASE=TRUE	TDM_SPKRAMP_L_D2R	
TDM_1V8_SPKRAMP_L_BCLK	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_L_BCLK	
TDM_1V8_SPKRAMP_L_FSYNC	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_L_FSYNC	
TDM_1V8_SPKRAMP_L_R2D	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_L_R2D	
TDM_1V8_SPKRAMP_L_D2R	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_L_D2R	
TDM_SPKRAMP_R_BCLK	MAKE_BASE=TRUE	TDM_SPKRAMP_R_BCLK	
TDM_SPKRAMP_R_FSYNC	MAKE_BASE=TRUE	TDM_SPKRAMP_R_FSYNC	
TDM_SPKRAMP_R_R2D	MAKE_BASE=TRUE	TDM_SPKRAMP_R_R2D	
TDM_SPKRAMP_R_D2R	MAKE_BASE=TRUE	TDM_SPKRAMP_R_D2R	
TDM_1V8_SPKRAMP_R_BCLK	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_R_BCLK	
TDM_1V8_SPKRAMP_R_FSYNC	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_R_FSYNC	
TDM_1V8_SPKRAMP_R_R2D	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_R_R2D	
TDM_1V8_SPKRAMP_R_D2R	MAKE_BASE=TRUE	TDM_1V8_SPKRAMP_R_D2R	
TPT_WLAN_JTAG_TCK	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TCK	
TPT_WLAN_JTAG_TMS	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TMS	
TPT_WLAN_JTAG_TRSTN	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TRSTN	
TPT_WLAN_JTAG_TDI	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TDI	
TPT_WLAN_JTAG_TDO	MAKE_BASE=TRUE	TPT_WLAN_JTAG_TDO	
TPT_P3V8AON_PU_RAIL	MAKE_BASE=TRUE	TPT_P3V8AON_PU_RAIL	

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6	NC_FPWM2	MAKE_BASE=TRUE	NO_TEST=1	NC_FPWM2
6	NC_SWD_TMS3	MAKE_BASE=TRUE	NO_TEST=1	NC_SWD_TMS3
6	NC_SWD_TMS4	MAKE_BASE=TRUE	NO_TEST=1	NC_SWD_TMS4
7	NC_I2S3_BCLK	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S3_BCLK
7	NC_I2S3_D2R	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S3_D2R
7	NC_I2S3_LRCLK	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S3_LRCLK
7	NC_I2S3_MCLK	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S3_MCLK
7	NC_I2S3_R2D	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S3_R2D
7	NC_SOC_GPIO01	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_GPIO01
7	IPD_SPI_EN	MAKE_BASE=TRUE	NO_TEST=1	IPD_SPI_EN
7	NC_SOC_GPIO09	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_GPIO09
7	NC_SOC_GPIO10	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_GPIO10
7	NC_SOC_GPIO15	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_GPIO15
7	NC_SOC_GPIO16	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_GPIO16
7	NC_SOC_I2S0_MCK	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_I2S0_MCK
7	NC_SOC_I2S1_MCK	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_I2S1_MCK
7	NC_SOC_I2S2_MCK	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_I2S2_MCK
7	NC_SOC_SPI2_SSIN	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_SPI2_SSIN
7	NC_SPMI2_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_SPMI2_CLK
7	NC_SPMI2_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_SPMI2_DATA
7	NC_SSPI0_MOSI	MAKE_BASE=TRUE	NO_TEST=1	NC_SSPI0_MOSI
7	NC_UART3_D2R	MAKE_BASE=TRUE	NO_TEST=1	NC_UART3_D2R
7	NC_UART3_D2R_CTS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_UART3_D2R_CTS_L
7	NC_UART3_R2D	MAKE_BASE=TRUE	NO_TEST=1	NC_UART3_R2D
7	NC_UART3_R2D_RTS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_UART3_R2D_RTS_L
7	NC_UART4_D2R	MAKE_BASE=TRUE	NO_TEST=1	NC_UART4_D2R
7	NC_UART4_D2R_CTS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_UART4_D2R_CTS_L
7	NC_UART4_R2D	MAKE_BASE=TRUE	NO_TEST=1	NC_UART4_R2D
7	NC_UART4_R2D_RTS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_UART4_R2D_RTS_L
7	NC_UART7_RXD	MAKE_BASE=TRUE	NO_TEST=1	NC_UART7_RXD
7	NC_UART7_TXD	MAKE_BASE=TRUE	NO_TEST=1	NC_UART7_TXD
8	NC_DISP_FSYNC	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_FSYNC
8	NC_DISP_SPMI_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_SPMI_CLK
8	NC_DISP_SPMI_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_SPMI_DATA
8	NC_DISP_TOUCH_BSYNC0	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_TOUCH_BSYNC0
8	NC_DISP_TOUCH_BSYNC1	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_TOUCH_BSYNC1
8	NC_DISP_TOUCH_EB	MAKE_BASE=TRUE	NO_TEST=1	NC_DISP_TOUCH_EB
8	NC_DISPLAY_POL	MAKE_BASE=TRUE	NO_TEST=1	NC_DISPLAY_POL
8	NC_ISP_GPIO1	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_GPIO1
8	NC_ISP_GPIO2	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_GPIO2
8	NC_ISP_GPIO3	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_GPIO3
8	NC_ISP_I2C0_SCL	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C0_SCL
8	NC_ISP_I2C0_SDA	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C0_SDA
8	NC_ISP_I2C1_SCL	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C1_SCL
8	NC_ISP_I2C1_SDA	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C1_SDA
8	NC_ISP_I2C3_SCL	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C3_SCL
8	NC_ISP_I2C3_SDA	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_I2C3_SDA
8	NC_ISP_SPMI0_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_SPMI0_CLK
8	NC_ISP_SPMI0_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_SPMI0_DATA
8	NC_ISP_SPMI1_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_SPMI1_CLK
8	NC_ISP_SPMI1_DATA	MAKE_BASE=TRUE	NO_TEST=1	NC_ISP_SPMI1_DATA
8	NC_LPDP_TX4N	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDP_TX4N
8	NC_LPDP_TX4P	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDP_TX4P
8	NC_LPDP_TX5N	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDP_TX5N
8	NC_LPDP_TX5P	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDP_TX5P
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9	NC_LPDPRX_AUX1	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX1
9	NC_LPDPRX_AUX2	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX2
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9	NC_LPDPRX_AUX4	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX4
9	NC_LPDPRX_AUX5	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX5
9	NC_LPDPRX_AUX6	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX6
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9	NC_LPDPRX_AUX9	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX9
9	NC_LPDPRX_AUX10	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX10
9	NC_LPDPRX_AUX11	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_AUX11
9	NC_MIPI0C_CLKN	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_CLKN
9	NC_MIPI0C_CLKP	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_CLKP
9	NC_MIPI0C_DATAN0	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_DATAN0
9	NC_MIPI0C_DATAN1	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_DATAN1
9	NC_MIPI0C_DATAP0	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_DATAP0
9	NC_MIPI0C_DATAP1	MAKE_BASE=TRUE	NO_TEST=1	NC_MIPI0C_DATAP1
9	NC_SENSOR0_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_SENSOR0_CLK
9	NC_SENSOR1_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_SENSOR1_CLK
9	NC_SENSOR2_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_SENSOR2_CLK
9	NC_SENSOR3_CLK	MAKE_BASE=TRUE	NO_TEST=1	NC_SENSOR3_CLK
9	NC_NAND0_PCIE_RESET1_L	MAKE_BASE=TRUE	NO_TEST=1	NC_NAND0_PCIE_RESET1_L
9	NC_PAD_MTR_ANALOG_TEST_NEG	MAKE_BASE=TRUE	NO_TEST=1	NC_PAD_MTR_ANALOG_TEST_NEG
9	NC_PAD_MTR_ANALOG_TEST_POS	MAKE_BASE=TRUE	NO_TEST=1	NC_PAD_MTR_ANALOG_TEST_POS
9	NC_PAD_MTR_VREF_NEG	MAKE_BASE=TRUE	NO_TEST=1	NC_PAD_MTR_VREF_NEG
9	NC_PAD_MTR_VREF_POS	MAKE_BASE=TRUE	NO_TEST=1	NC_PAD_MTR_VREF_POS
10	NC_AON_SLEEP1_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_AON_SLEEP1_RESET_L
10	NC_AOP_FUNC1	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC1
10	NC_AOP_FUNC5	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC5
10	NC_AOP_FUNC10	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC10
10	NC_AOP_FUNC14	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_FUNC14
10	NC_AOP_SPMI0_SCLK	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_SPMI0_SCLK
10	NC_AOP_SPMI0_SDATA	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_SPMI0_SDATA
10	NC_AOP_UART2_D2R	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_UART2_D2R
10	NC_AOP_UART2_R2D	MAKE_BASE=TRUE	NO_TEST=1	NC_AOP_UART2_R2D

10	NC_PDM_CLK1	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_CLK1
10	NC_PDM_CLK2	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_CLK2
10	NC_PDM_CLK5	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_CLK5
10	NC_PDM_CLK6	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_CLK6
10	NC_PDM_DATA1	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_DATA1
10	NC_PDM_DATA2	MAKE_BASE=TRUE	NO_TEST=1	NC_PDM_DATA2
16	NC_SMC_GPIO1	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_GPIO1

23	NC_CHGR_CBC_ON	MAKE_BASE=TRUE	NO_TEST=1	NC_CHGR_CBC_ON
23	NC_CHGR_EN_VR1	MAKE_BASE=TRUE	NO_TEST=1	NC_CHGR_EN_VR1
23	NC_CHGR_SMC_RST_L	MAKE_BASE=TRUE	NO_TEST=1	NC_CHGR_SMC_RST_L
56	NC_EUSB_LS1N	MAKE_BASE=TRUE	NO_TEST=1	NC_EUSB_LS1N
56	NC_EUSB_LS1P	MAKE_BASE=TRUE		NC_EUSB_LS1P
21	NC_SE_GPIO0	MAKE_BASE=TRUE	NO_TEST=1	NC_SE_GPIO0
51	NC_SMBUS_ATCRTMR0_SCL	MAKE_BASE=TRUE	NO_TEST=1	NC_SMBUS_ATCRTMR0_SCL
51	NC_SMBUS_ATCRTMR0_SDA	MAKE_BASE=TRUE	NO_TEST=1	NC_SMBUS_ATCRTMR0_SDA
52	NC_SMBUS_ATCRTMR1_SCL	MAKE_BASE=TRUE	NO_TEST=1	NC_SMBUS_ATCRTMR1_SCL
52	NC_SMBUS_ATCRTMR1_SDA	MAKE_BASE=TRUE	NO_TEST=1	NC_SMBUS_ATCRTMR1_SDA
58	NC_USB_LS1N	MAKE_BASE=TRUE	NO_TEST=1	NC_USB_LS1N
58	NC_USB_LS1P	MAKE_BASE=TRUE	NO_TEST=1	NC_USB_LS1P
8	NC_LPDPRX_RXN0	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN0
8	NC_LPDPRX_RXN1	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN1
8	NC_LPDPRX_RXN2	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN2
8	NC_LPDPRX_RXN3	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN3
8	NC_LPDPRX_RXN4	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN4
8	NC_LPDPRX_RXN5	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN5
8	NC_LPDPRX_RXN6	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN6
8	NC_LPDPRX_RXN7	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN7
8	NC_LPDPRX_RXN8	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN8
8	NC_LPDPRX_RXN9	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN9
8	NC_LPDPRX_RXN10	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN10
8	NC_LPDPRX_RXN11	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXN11
8	NC_LPDPRX_RXP0	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP0
8	NC_LPDPRX_RXP1	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP1
8	NC_LPDPRX_RXP2	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP2
8	NC_LPDPRX_RXP3	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP3
8	NC_LPDPRX_RXP4	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP4
8	NC_LPDPRX_RXP5	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP5
8	NC_LPDPRX_RXP6	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP6
8	NC_LPDPRX_RXP7	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP7
8	NC_LPDPRX_RXP8	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP8
8	NC_LPDPRX_RXP9	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP9
8	NC_LPDPRX_RXP10	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP10
8	NC_LPDPRX_RXP11	MAKE_BASE=TRUE	NO_TEST=1	NC_LPDPRX_RXP11
62	NC_NAND0_S5E0_VPP	MAKE_BASE=TRUE	NO_TEST=1	NC_NAND0_S5E0_VPP
63	NC_NAND0_S5E1_VPP	MAKE_BASE=TRUE	NO_TEST=1	NC_NAND0_S5E1_VPP

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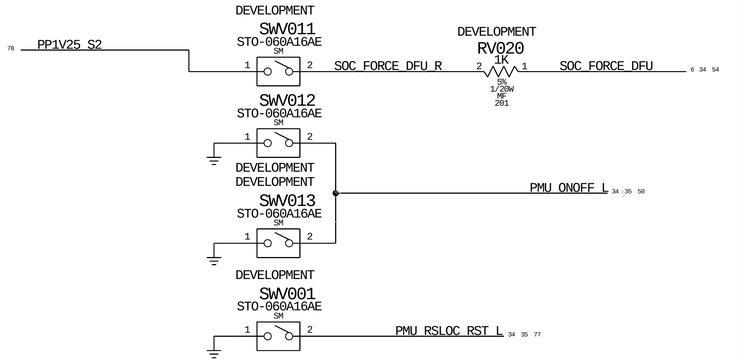
A Debug Push-Buttons



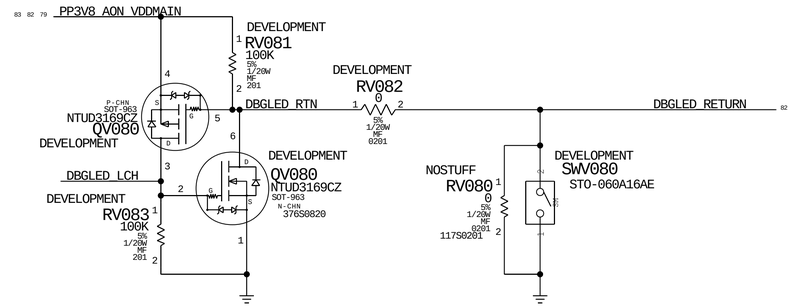
B Debug LED Control

Debug LED Latch

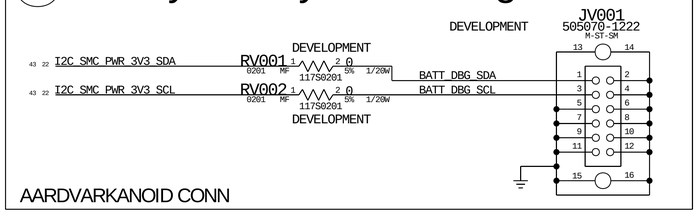
Press button once to engage.

Remove power to disengage.

Debug LED Enable

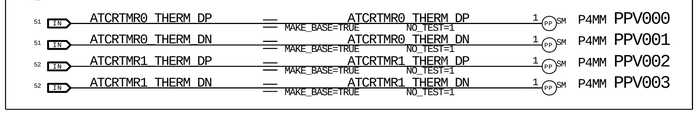


C Battery Sub-System Debug Connector



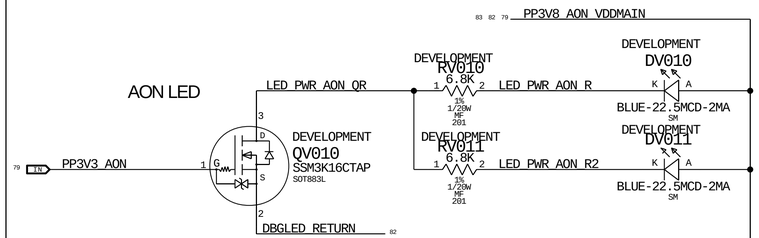
AARDVARKANOID CONN

D Thermal Diode Test Points

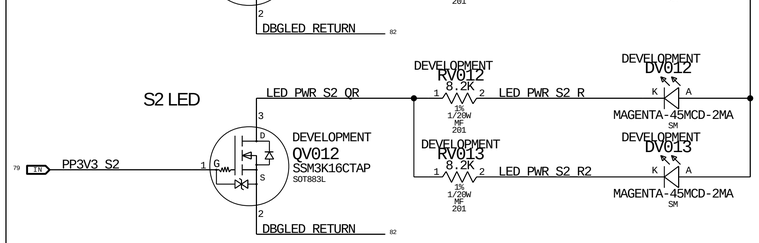


E Debug LEDs

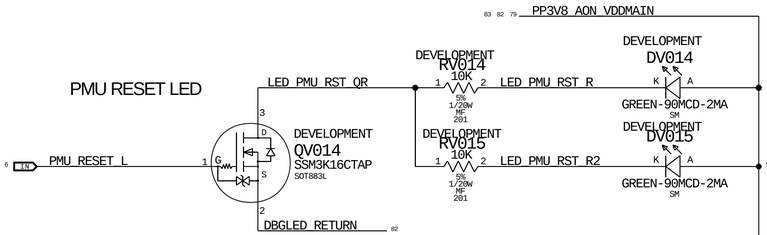
AON LED



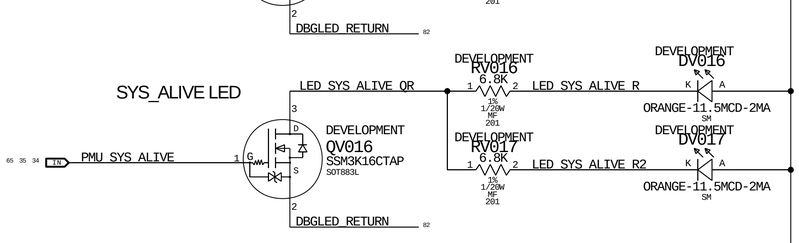
S2 LED



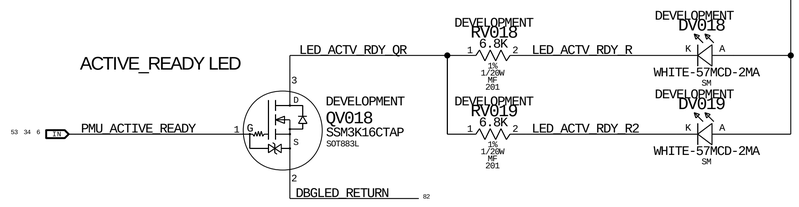
PMU RESET LED



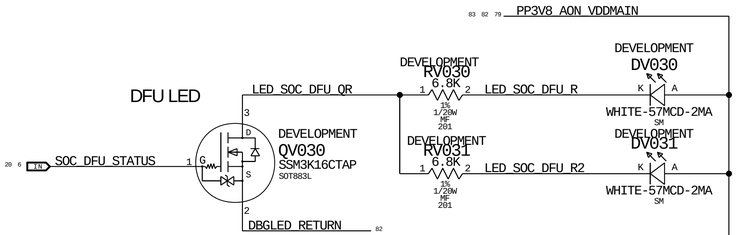
SYS_ALIVE LED



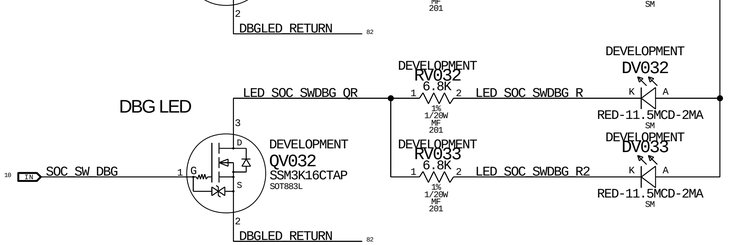
ACTIVE_READY LED



DFU LED



DBG LED



BOM_COST_GROUP=DEBUG

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PP3V8_AON_VDDMAIN

CW100 12PF 5% 25V NP0-C0G 0201
CW101 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW102 12PF 5% 25V NP0-C0G 0201
CW103 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW104 12PF 5% 25V NP0-C0G 0201
CW105 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW106 12PF 5% 25V NP0-C0G 0201
CW107 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW108 12PF 5% 25V NP0-C0G 0201
CW109 3.0PF +/-0.1PF 25V NP0-C0G 0201

CW10B 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW10C 12PF 5% 25V NP0-C0G 0201
CW10D 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW10E 12PF 5% 25V NP0-C0G 0201
CW10F 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW116 12PF 5% 25V NP0-C0G 0201

CW11A 12PF 5% 25V NP0-C0G 0201
CW11B 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW11C 12PF 5% 25V NP0-C0G 0201
CW11E 12PF 5% 25V NP0-C0G 0201
CW11F 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW122 12PF 5% 25V NP0-C0G 0201
CW123 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW124 12PF 5% 25V NP0-C0G 0201
CW125 3.0PF +/-0.1PF 25V NP0-C0G 0201

PPBUS_AON

CW136 12PF 5% 25V NP0-C0G 0201
CW137 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW138 12PF 5% 25V NP0-C0G 0201
CW139 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW13A 12PF 5% 25V NP0-C0G 0201
CW13B 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW13C 12PF 5% 25V NP0-C0G 0201
CW13D 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW13E 12PF 5% 25V NP0-C0G 0201
CW13F 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW117 12PF 5% 25V NP0-C0G 0201
CW118 12PF 5% 25V NP0-C0G 0201
CW119 12PF 5% 25V NP0-C0G 0201

PPVOUT_LCDBKLT

CW18A 12PF 5% 100V C0G 0201
CW18B 3PF +/-0.1PF 100V C0G 0201
CW18C 12PF 5% 100V C0G 0201
CW18D 3PF +/-0.1PF 100V C0G 0201
CW18E 12PF 5% 100V C0G 0201
CW18F 3PF +/-0.1PF 100V C0G 0201
CW194 12PF 5% 100V C0G 0201
CW195 3PF +/-0.1PF 100V C0G 0201
CW196 12PF 5% 100V C0G 0201
CW197 3PF +/-0.1PF 100V C0G 0201

PPVOUT_LCDBKLT_SW

CW198 12PF 5% 100V C0G 0201
CW199 3PF +/-0.1PF 100V C0G 0201

PPVIN_LCDBKLT_O

CW19A 12PF 5% 100V C0G 0201
CW19B 3PF +/-0.1PF 100V C0G 0201
CW19C 12PF 5% 100V C0G 0201
CW19D 3PF +/-0.1PF 100V C0G 0201
CW19E 12PF 5% 100V C0G 0201
CW19F 3PF +/-0.1PF 100V C0G 0201
CW1A8 12PF 5% 100V C0G 0201
CW1A9 3PF +/-0.1PF 100V C0G 0201

PP1V2_S2_CIO

CW110 12PF 5% 25V NP0-C0G 0201
CW111 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW112 12PF 5% 25V NP0-C0G 0201
CW113 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW114 12PF 5% 25V NP0-C0G 0201
CW115 3.0PF +/-0.1PF 25V NP0-C0G 0201

PPVOUT_KBDBKLT

CW1AA 12PF 5% 100V C0G 0201
CW1AB 3PF +/-0.1PF 100V C0G 0201
CW1AC 12PF 5% 100V C0G 0201
CW1AD 3PF +/-0.1PF 100V C0G 0201

PPVDD_DISP_S1

CW130 12PF 5% 25V NP0-C0G 0201
CW131 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW132 12PF 5% 25V NP0-C0G 0201
CW133 12PF 5% 25V NP0-C0G 0201

PPVDD_ECPU_AWAKE

CW134 12PF 5% 25V NP0-C0G 0201
CW135 3.0PF +/-0.1PF 25V NP0-C0G 0201

PPVDD_GPU_AWAKE

CW126 12PF 5% 25V NP0-C0G 0201
CW127 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP1V2_AWAKE_PLL

CW120 12PF 5% 25V NP0-C0G 0201
CW121 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP1V25_AWAKE_IO

CW140 12PF 5% 25V NP0-C0G 0201
CW141 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW142 12PF 5% 25V NP0-C0G 0201
CW143 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP5V_S2

CW1C3 12PF 5% 25V NP0-C0G 0201
CW1C4 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW1C5 12PF 5% 25V NP0-C0G 0201
CW1C6 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP0V805_S1_VDD_FIXED

CW146 12PF 5% 25V NP0-C0G 0201

P5VS2_SW

CW1C7 12PF 5% 25V NP0-C0G 0201
CW1C8 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW1C9 12PF 5% 25V NP0-C0G 0201
CW1CA 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP5V_S2_KBDLED

CW1CB 12PF 5% 25V NP0-C0G 0201
CW1CC 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP0V6_S1_VDDQL

CW150 12PF 5% 25V NP0-C0G 0201
CW151 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW152 12PF 5% 25V NP0-C0G 0201
CW153 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW154 12PF 5% 25V NP0-C0G 0201
CW155 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW15A 12PF 5% 25V NP0-C0G 0201
CW15B 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW15C 12PF 5% 25V NP0-C0G 0201
CW15D 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW15E 12PF 5% 25V NP0-C0G 0201
CW15F 3.0PF +/-0.1PF 25V NP0-C0G 0201

PPVDD_ECPU_AWAKE

CW156 12PF 5% 25V NP0-C0G 0201

PP2V5_NAND0_DISCHARGE

CW160 12PF 5% 25V NP0-C0G 0201
CW161 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP2V5_AWAKE_NAND

CW170 12PF 5% 25V NP0-C0G 0201
CW171 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW172 12PF 5% 25V NP0-C0G 0201
CW173 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW174 12PF 5% 25V NP0-C0G 0201
CW175 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW176 12PF 5% 25V NP0-C0G 0201
CW177 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW178 12PF 5% 25V NP0-C0G 0201
CW179 3.0PF +/-0.1PF 25V NP0-C0G 0201

CW180 12PF 5% 25V NP0-C0G 0201
CW181 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW182 12PF 5% 25V NP0-C0G 0201
CW183 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW184 12PF 5% 25V NP0-C0G 0201
CW185 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW186 12PF 5% 25V NP0-C0G 0201
CW187 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW188 12PF 5% 25V NP0-C0G 0201
CW189 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP1V25_AWAKE_NAND

CW190 12PF 5% 25V NP0-C0G 0201
CW191 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW192 12PF 5% 25V NP0-C0G 0201
CW193 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP0V88_AWAKE_NAND

CW1A0 12PF 5% 25V NP0-C0G 0201
CW1A1 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW1A2 12PF 5% 25V NP0-C0G 0201
CW1A3 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW1A4 12PF 5% 25V NP0-C0G 0201
CW1A5 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW1A6 12PF 5% 25V NP0-C0G 0201
CW1A7 3.0PF +/-0.1PF 25V NP0-C0G 0201

PPVDD_SOC_S1

CW1B0 12PF 5% 25V NP0-C0G 0201

PP1V06_S2SW_DRAM

CW1B6 12PF 5% 25V NP0-C0G 0201
CW1B7 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW1B8 12PF 5% 25V NP0-C0G 0201
CW1BA 12PF 5% 25V NP0-C0G 0201
CW1BB 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW1BC 12PF 5% 25V NP0-C0G 0201
CW1BD 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW1BE 12PF 5% 25V NP0-C0G 0201
CW1BF 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP0V72_S2_VDD_LOW

CW1C0 12PF 5% 25V NP0-C0G 0201
CW1C1 3.0PF +/-0.1PF 25V NP0-C0G 0201

P3V8AON_VSW1

CW162 12PF 5% 25V NP0-C0G 0201
CW163 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP3V8AON_PH1

CW164 12PF 5% 25V NP0-C0G 0201

PPBUS_AON_L_SPKRAMP

CW147 12PF 5% 25V NP0-C0G 0201
CW148 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW149 12PF 5% 25V NP0-C0G 0201
CW14A 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW14B 12PF 5% 25V NP0-C0G 0201
CW14C 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW14D 12PF 5% 25V NP0-C0G 0201
CW145 3.0PF +/-0.1PF 25V NP0-C0G 0201

P3V8AON_SW2

CW166 12PF 5% 25V NP0-C0G 0201
CW167 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW168 12PF 5% 25V NP0-C0G 0201
CW169 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP3V8AON_PH2

CW16B 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW16C 12PF 5% 25V NP0-C0G 0201

P3V8AON_SW3

CW16E 12PF 5% 25V NP0-C0G 0201
CW16F 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW17A 12PF 5% 25V NP0-C0G 0201
CW17B 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP3V8AON_PH3

CW17C 12PF 5% 25V NP0-C0G 0201
CW17D 3.0PF +/-0.1PF 25V NP0-C0G 0201
CW17E 12PF 5% 25V NP0-C0G 0201

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SCSET RULES

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_(N)K Calculates dielectric distance from stackup electrical distance to next metal, "x" is defined	EXAMPLE: 3.5,6,7x,8x,10x 2-10
A_DIELECTRIC_(N)XD XV,VVL,X Calculate dielectric distance from metal this and electrical distance to next metal, "x" is defined	EXAMPLE: 2.5X,10-50,7V,8V,10V PLEASE USE HYBRID TABLE
A_DIELECTRIC_(N)XIN_(N)XOUT Calculate dielectric distance from stackup electrical distance to next metal, "x" is defined	EXAMPLE: 3.5,6,8x

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PHYSICAL CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLOCK ASSIGNED
CLASS NAME	(P,S,I)	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
I2C	P	A_45_OHM_SE	*SMB*SCL*,*SMB*SDA*,*I2C*SCL*,*I2C*SDA*,*I2C*INT*	Y
SPI	P	A_45_OHM_SE	*SPI*MISO*,*SPI*MOSI*,*SPI*CLK*,*SPI*CS*	Y
SPMI	P	A_45_OHM_SE	*SPMI*	Y
SWD	P	A_45_OHM_SE	SWD_NAND*,SWD_NUB*	Y
JTAG	P	A_45_OHM_SE	*JTAG*SEL,*JTAG*TCK,*JTAG*TDI,*JTAG*TDO,*JTAG*TMS	Y
CLOCK_24M	P	A_45_OHM_SE	SOC_XTAL24M*,SOC_24M_O_R,NAND0_CLK24M*	Y
CLOCK_32K	P	A_45_OHM_SE	PMU_CLK32K*	Y
TDM_LEFT	P	A_45_OHM_SE	TDM_SPKRAMP_L*	Y
TDM_RIGHT	P	A_45_OHM_SE	TDM_SPKRAMP_R*	Y
TDM_CODEC	P	A_45_OHM_SE	TDM_CODEC*	Y
SPKR_ICC	P	A_45_OHM_SE	SPKRAMP_ICC,SPKRAMP_*_ICC_R	Y
UART	P	A_45_OHM_SE	UART_*	Y
RESETS	P	A_45_OHM_SE	*RST*,*RESET*,*PERST*	Y
WDOG	P	A_45_OHM_SE	SOC_WDOG	Y
SOCHOT	P	A_45_OHM_SE	SOC_SOCHOT_L	Y
POWER_BUTTON	P	A_45_OHM_SE	*PMU_ONOFF*	Y
FAULT	P	A_45_OHM_SE	*FAULT*	Y
DMIC_PDM	P	A_45_OHM_SE	PDM_DMIC_DATA*,DMIC_DATA*,PDM_DMIC_CLK*,DMIC_CLK*	Y
CIO_D2R	P	A_85_OHM_DIFF	DP:DP_USBC*_D2R*	Y
CIO_R2D	P	A_85_OHM_DIFF	DP:DP_USBC*_R2D*	Y
PCIE_NAND_D2R	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND*_D2R*	Y
PCIE_NAND_R2D	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND*_R2D*	Y
PCIE_WLBT_D2R	P	A_85_OHM_DIFF	DP:DP_PCIE_WLBT*_R2D*	Y
PCIE_WLBT_R2D	P	A_85_OHM_DIFF	DP:DP_PCIE_WLBT*_D2R*	Y
LPDP	P	A_85_OHM_DIFF	DP:DP_LPDP_INT_DATA*	Y
PCIE_CLK	P	A_85_OHM_DIFF	DP:DP_PCIE_CLK100M*	Y
PCIE_CLKREQ	P	A_45_OHM_SE	*CLKREQ*	Y
MIPI_CLK	P	A_85_OHM_DIFF	DP:DP_MIPI_FTCAM_CLK*,DP_MIPI_CLOCK*	Y
MIPI_DATA	P	A_85_OHM_DIFF	DP:DP_MIPI_FTCAM_DATA*,DP_MIPI_DATA*	Y
EUSB	P	A_85_OHM_DIFF	DP:DP_EUSB*	Y
GROUND	P	DEFAULT	GND	Y
POWER	P	POWER	PP*	Y

PHYSICAL CONSTRAINT SET, NET ASSIGNMENT

(P,S,I)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)

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17.2 PHYSICAL CSETS

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SPACING CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR ASSIGNED
CLASS NAME	***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
CLOCK_24M	S	A_DIELECTRIC_3X	=	Y
CLOCK_32K	S	A_DIELECTRIC_3X	=	Y
CIO_D2R	S	A_DIELECTRIC_9X	=	Y
CIO_R2D	S	A_DIELECTRIC_9X	=	Y
PCIE_NAND_D2R	S	A_DIELECTRIC_9X	=	Y
PCIE_NAND_R2D	S	A_DIELECTRIC_9X	=	Y
PCIE_WLBT_D2R	S	A_DIELECTRIC_7X	=	Y
PCIE_WLBT_R2D	S	A_DIELECTRIC_7X	=	Y
PCIE_CLK	S	A_DIELECTRIC_6X	=	Y
LPDP	S	A_DIELECTRIC_6X	=	Y
MIPI_CLK	S	A_DIELECTRIC_5X	=	Y
MIPI_DATA	S	A_DIELECTRIC_5X	=	Y
EUSB	S	A_DIELECTRIC_5X	=	Y
GROUND	S	DEFAULT	=	Y
POWER	S	DEFAULT	=	Y
RF	S	RF	RF_ANT*	Y

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17.2 SPACING CSETS, ISO

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SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
CIO_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
CIO_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
LPDP	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_CLK	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
MIPI_DATA	GROUND	DEFAULT_WITH_4X_TO_SHAPE
MIPI_CLK	GROUND	DEFAULT_WITH_4X_TO_SHAPE
CIO_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
CIO_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
LPDP	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_CLK	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
MIPI_DATA	POWER	DEFAULT_WITH_4X_TO_SHAPE
MIPI_CLK	POWER	DEFAULT_WITH_4X_TO_SHAPE
CIO_D2R	CIO_D2R	A_DIELECTRIC_4X
CIO_D2R	PCIE_NAND_D2R	A_DIELECTRIC_4X
CIO_D2R	PCIE_WLBT_D2R	A_DIELECTRIC_4X
CIO_D2R	MIPI_CLK	A_DIELECTRIC_4X
CIO_D2R	MIPI_DATA	A_DIELECTRIC_4X
CIO_D2R	CIO_R2D	A_DIELECTRIC_7X
PCIE_NAND_D2R	PCIE_NAND_D2R	A_DIELECTRIC_4X
PCIE_NAND_D2R	PCIE_WLBT_D2R	A_DIELECTRIC_4X
PCIE_NAND_D2R	MIPI_DATA	A_DIELECTRIC_4X
PCIE_NAND_D2R	MIPI_CLK	A_DIELECTRIC_4X
PCIE_NAND_D2R	PCIE_NAND_R2D	A_DIELECTRIC_7X
PCIE_WLBT_D2R	PCIE_WLBT_R2D	A_DIELECTRIC_4X
PCIE_WLBT_D2R	MIPI_DATA	A_DIELECTRIC_4X
PCIE_WLBT_D2R	MIPI_CLK	A_DIELECTRIC_4X
MIPI_DATA	MIPI_CLK	A_DIELECTRIC_2X
CIO_R2D	CIO_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_NAND_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_WLBT_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_CLK	A_DIELECTRIC_4X
CIO_R2D	LPDP	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_NAND_R2D	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_WLBT_R2D	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_CLK	A_DIELECTRIC_4X
PCIE_NAND_R2D	LPDP	A_DIELECTRIC_4X
PCIE_WLBT_R2D	PCIE_CLK	A_DIELECTRIC_4X
PCIE_WLBT_R2D	LPDP	A_DIELECTRIC_4X
PCIE_CLK	PCIE_CLK	A_DIELECTRIC_4X
PCIE_CLK	LPDP	A_DIELECTRIC_4X
LPDP	LPDP	A_DIELECTRIC_3X

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CPU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
939-08813	1	PCBA,KANHA,X1711	U0600	CRITICAL	CPU:INTERPOSER

A1 BEST

998-21412	1	SOC,TGA A1+8G,1Y,8C,DEV,CX,H,ATK,MCM2502			U0600	CRITICAL	CPU:SOC_A1_HYNIX_8GB_BEST
998-21413	998-21412	CPU:SOC_A1_HYNIX_8GB_BEST	ALL	SCK			
998-21414	1	SOC,TGA A1+8G,1Y,8C,DEV,CX,M,ATK,MCM2502			U0600	CRITICAL	CPU:SOC_A1_MICRON_8GB_BEST
998-21415	998-21414	CPU:SOC_A1_MICRON_8GB_BEST	ALL	SCK			
998-21416	1	SOC,TGA A1+16G,1Y,8C,DEV,DX,H,ATK,MC2502			U0600	CRITICAL	CPU:SOC_A1_HYNIX_16GB_BEST
998-21417	998-21416	CPU:SOC_A1_HYNIX_16GB_BEST	ALL	SCK			
998-21418	1	SOC,TGA A1+16G,1X,8C,DEV,DX,M,ATK,MC2502			U0600	CRITICAL	CPU:SOC_A1_MICRON_16GB_BEST
998-21420	998-21418	CPU:SOC_A1_MICRON_16GB_BEST	ALL	SCK			

A1 GOOD

998-21421	1	SOC,TGA A1+8G,1Y,7C,DEV,CX,H,ATK,MCM2502			U0600	CRITICAL	CPU:SOC_A1_HYNIX_8GB_GOOD
998-21422	998-21421	CPU:SOC_A1_HYNIX_8GB_GOOD	ALL	SCK			
998-21412	998-21421	CPU:SOC_A1_HYNIX_8GB_GOOD	ALL	ACK			
998-21413	998-21421	CPU:SOC_A1_HYNIX_8GB_GOOD	ALL	SCK			
998-21423	1	SOC,TGA A1+8G,1Y,7C,DEV,CX,M,ATK,MCM2502			U0600	CRITICAL	CPU:SOC_A1_MICRON_8GB_GOOD
998-21424	998-21423	CPU:SOC_A1_MICRON_8GB_GOOD	ALL	SCK			
998-21414	998-21423	CPU:SOC_A1_MICRON_8GB_GOOD	ALL	ACK			
998-21415	998-21423	CPU:SOC_A1_MICRON_8GB_GOOD	ALL	SCK			
998-21426	1	SOC,TGA A1+16G,1Y,7C,DEV,DX,H,ATK,MC2502			U0600	CRITICAL	CPU:SOC_A1_HYNIX_16GB_GOOD
998-21427	998-21426	CPU:SOC_A1_HYNIX_16GB_GOOD	ALL	SCK			
998-21416	998-21426	CPU:SOC_A1_HYNIX_16GB_GOOD	ALL	ACK			
998-21417	998-21426	CPU:SOC_A1_HYNIX_16GB_GOOD	ALL	SCK			
998-21428	1	SOC,TGA A1+16G,1X,7C,DEV,DX,M,ATK,MC2502			U0600	CRITICAL	CPU:SOC_A1_MICRON_16GB_GOOD
998-21429	998-21428	CPU:SOC_A1_MICRON_16GB_GOOD	ALL	SCK			
998-21418	998-21428	CPU:SOC_A1_MICRON_16GB_GOOD	ALL	ACK			
998-21420	998-21428	CPU:SOC_A1_MICRON_16GB_GOOD	ALL	SCK			

B0 BEST

998-22388	1	SOC,TGA B0+8G,1Y,8C,LP,DEV,CX,H,A,M2502			U0600	CRITICAL	CPU:SOC_HYNIX_8GB_BEST
998-22387	998-22388	CPU:SOC_HYNIX_8GB_BEST	ALL	SCK			
998-22386	1	SOC,TGA B0+8G,1Y,8C,LP,DEV,CX,M,A,M2502			U0600	CRITICAL	CPU:SOC_MICRON_8GB_BEST
998-22385	998-22386	CPU:SOC_MICRON_8GB_BEST	ALL	SCK			
998-22392	1	SOC,TGA B0+16G,1Y,8C,LP,DEV,DX,H,A,M2502			U0600	CRITICAL	CPU:SOC_HYNIX_16GB_BEST
998-22391	998-22392	CPU:SOC_HYNIX_16GB_BEST	ALL	SCK			
998-22390	1	SOC,TGA B0+16G,1X,8C,LP,DEV,DX,M,A,M2502			U0600	CRITICAL	CPU:SOC_MICRON_16GB_BEST
998-22389	998-22390	CPU:SOC_MICRON_16GB_BEST	ALL	SCK			

B0 GOOD

998-22404	1	SOC,TGA B0+8G,1Y,7C,LP,DEV,CX,H,A,M2502			U0600	CRITICAL	CPU:SOC_HYNIX_8GB_GOOD
998-22403	998-22404	CPU:SOC_HYNIX_8GB_GOOD	ALL	SCK			
998-22388	998-22404	CPU:SOC_HYNIX_8GB_GOOD	ALL	ACK			
998-22387	998-22404	CPU:SOC_HYNIX_8GB_GOOD	ALL	SCK			
998-22402	1	SOC,TGA B0+8G,1Y,7C,LP,DEV,CX,M,A,M2502			U0600	CRITICAL	CPU:SOC_MICRON_8GB_GOOD
998-22401	998-22402	CPU:SOC_MICRON_8GB_GOOD	ALL	SCK			
998-22386	998-22402	CPU:SOC_MICRON_8GB_GOOD	ALL	ACK			
998-22385	998-22402	CPU:SOC_MICRON_8GB_GOOD	ALL	SCK			
998-22409	1	SOC,TGA B0+16G,1Y,7C,LP,DEV,DX,H,A,M2502			U0600	CRITICAL	CPU:SOC_HYNIX_16GB_GOOD
998-22408	998-22409	CPU:SOC_HYNIX_16GB_GOOD	ALL	SCK			
998-22392	998-22409	CPU:SOC_HYNIX_16GB_GOOD	ALL	ACK			
998-22391	998-22409	CPU:SOC_HYNIX_16GB_GOOD	ALL	SCK			
998-22407	1	SOC,TGA B0+16G,1X,7C,LP,DEV,DX,M,A,M2502			U0600	CRITICAL	CPU:SOC_MICRON_16GB_GOOD
998-22406	998-22407	CPU:SOC_MICRON_16GB_GOOD	ALL	SCK			
998-22390	998-22407	CPU:SOC_MICRON_16GB_GOOD	ALL	ACK			
998-22389	998-22407	CPU:SOC_MICRON_16GB_GOOD	ALL	SCK			

NAND Landing 0

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-18368	1	IC,NAND,SSE MCP ROUTING STUDY,LGA110	UN000	CRITICAL	NAND_L0:SSE_STUDY
335S00462	1	NAND,3DV4,128GBT,XXX,SSE,256G,T,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_128G_TO
335S00470	1	NAND,3DV4,128GBT,XXX,SSE,256G,SD,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_128G_SD
335S00437	1	NAND,3DV5,128GB,SSE,512G,H,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_256G_HY
335S00489	1	NAND,3DV4,160GBT,XXX,SSE,256G,SD,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_256G_SD
335S00480	1	NAND,3DV4,160GBT,XXX,SSE,256G,K,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_256G_TO
335S00482	1	NAND,3DV5,320GB,SSE,512G,H,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_512G_HY
335S00481	1	NAND,3DV4,288GBT,XXX,SSE,256G,K,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_512G_TO
335S00474	1	NAND,3DV4,512GBT,XXX,SSE,256G,SD,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_1P0T_SD
335S00466	1	NAND,3DV4,512GBT,XXX,SSE,256G,T,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_1P0T_TO
335S00468	1	NAND,3DV4,1TBT,XXX,SSE,512G,T,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_2P0T_TO
335S00458	1	NAND,3DV5,1024GBT,SSE,512G,H,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_2P0T_HY
939-08815	1	PCBA,BANDIPUR,X1711	UN000	CRITICAL	NAND_L0:INTERPOSER

NAND Landing 1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-18368	1	IC,NAND,SSE MCP ROUTING STUDY,LGA110	UN100	CRITICAL	NAND_L1:SSE_STUDY
335S00437	1	NAND,3DV5,128GB,SSE,512G,H,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_256G_HY
335S00470	1	NAND,3DV4,128GBT,XXX,SSE,256G,SD,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_256G_SD
335S00462	1	NAND,3DV4,128GBT,XXX,SSE,256G,T,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_256G_TO
335S00438	1	NAND,3DV5,256GB,SSE,512G,H,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_512G_HY
335S00464	1	NAND,3DV4,256GBT,XXX,SSE,256G,T,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_512G_TO
335S00474	1	NAND,3DV4,512GBT,XXX,SSE,256G,SD,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_1P0T_SD
335S00466	1	NAND,3DV4,512GBT,XXX,SSE,256G,T,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_1P0T_TO
335S00468	1	NAND,3DV4,1TBT,XXX,SSE,512G,T,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_2P0T_TO
335S00458	1	NAND,3DV5,1024GBT,SSE,512G,H,SLGA110	UN100	CRITICAL	NAND_L1:ITLC_2P0T_HY
939-08815	1	PCBA,BANDIPUR,X1711	UN100	CRITICAL	NAND_L1:INTERPOSER

SPMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-20066	1	IC,PMU,SPMU,A0,OTP-JPC,WLCSP196	U7700	CRITICAL	SPMU_IC:DEV
998-22526	1	IC,PMU,SIMETRA,A1,OTP-JPE,WLCSP196	U7700	CRITICAL	SPMU_IC:A1

MPMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-20064	1	IC,PMU,MPMU,A0,OTP-JPE,WLCSP440	U8100	CRITICAL	MPMU_IC:DEV
998-22614	1	IC,PMU,SERA,B0,OTP-JPF,WLCSP440	U8100	CRITICAL	MPMU_IC:B0

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NAND BOM GROUPS

BOM GROUP	BOM OPTIONS
NANDCFG:ITLC_S5E_128G_TO	NAND_L0:ITLC_128G_TO
NANDCFG:ITLC_S5E_128G_SD	NAND_L0:ITLC_128G_SD
NANDCFG:ITLC_S5E_256G_HY	NAND_L0:ITLC_256G_HY,NAND_L1:ITLC_256G_HY,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_256G_SD	NAND_L0:ITLC_256G_SD,NAND_L1:ITLC_256G_SD,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_256G_TO	NAND_L0:ITLC_256G_TO,NAND_L1:ITLC_256G_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_512G_HY	NAND_L0:ITLC_512G_HY,NAND_L1:ITLC_512G_HY,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_512G_TO	NAND_L0:ITLC_512G_TO,NAND_L1:ITLC_512G_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_1P0T_SD	NAND_L0:ITLC_1P0T_SD,NAND_L1:ITLC_1P0T_SD,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_1P0T_TO	NAND_L0:ITLC_1P0T_TO,NAND_L1:ITLC_1P0T_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_2P0T_TO	NAND_L0:ITLC_2P0T_TO,NAND_L1:ITLC_2P0T_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_2P0T_HY	NAND_L0:ITLC_2P0T_HY,NAND_L1:ITLC_2P0T_HY,PARTS_SSDNAND1
NANDCFG:INTERPOSER	NAND_L0:INTERPOSER,NAND_L1:INTERPOSER,PARTS_SSDNAND1
NANDCFG:NONE	NAND_L0:OFF,NAND_L1:OFF,PARTS_SSDNAND1

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BOM GROUPS

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Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	Alternate Vendor	Primary Vendor
353S01346	353S01320		ALL	rdar://problem/57736570	On Semi	NXP
138S0738	138S1101		ALL	rdar://problem/59471401	Samsung	Murata
138S0846	138S0811		ALL	rdar://problem/59474499	Samsung	Murata
376S1053	376S0604		ALL	rdar://problem/59475163	Diodes Inc	On Semi
152S00359	152S00253		ALL	rdar://problem/57204466	Chilisin	Cyntec
740S00041	740S0159		ALL	rdar://problem/59438907	Bourns	LittleFuse
371S00077	371S00180		ALL	rdar://problem/59475330	NXP	Diodes Inc
376S1106	376S0678		ALL	rdar://problem/59442581	On Semi	Vishay
107S00033	107S00034		ALL	rdar://problem/59471007	TFT	Cyntec
138S00087	138S1086		ALL	rdar://problem/59439865	Taiyo Yuden	Murata
152S00812	152S1701		ALL	rdar://problem/59465659	Chilisin	Cyntec
371S00217	371S00079		ALL	rdar://problem/57739774	ROHM CORP	Nexperia
376S0948	376S00076		ALL	rdar://problem/59134310	Diodes Inc	Toshiba
128S00031	128S00011		ALL	rdar://problem/59071370	ROHM CORP	Kemet
128S00026	128S00011		ALL	rdar://problem/59071370	NEC/Kemet	Kemet
128S00087	128S00011		ALL	rdar://problem/59071370	Panasonic	Kemet
128S0445	128S0436		ALL	rdar://problem/59071568	Panasonic	Kemet
128S0364	128S0264		ALL	rdar://problem/59071705	Kemet	Panasonic
128S00094	128S00067		ALL	rdar://problem/59072397	Tokin/Kemet	Panasonic
128S00039	128S00038		ALL	rdar://problem/59075402	NEC/Kemet	Kemet
128S0382	128S00038		ALL	rdar://problem/59075402	Panasonic	Kemet
152S00680	152S00198		ALL	rdar://problem/59075547	Chilisin	Cyntec
152S00383	152S00198		ALL	rdar://problem/59075547	Vishay	Cyntec
152S00708	152S00265		ALL	rdar://problem/59075783	Chilisin	Cyntec
152S00367	152S01248		ALL	rdar://problem/59076041	NEC	Cyntec
376S00204	376S00203		ALL	rdar://problem/59076791	Diodes Inc	Vishay
376S00226	376S00203		ALL	rdar://problem/59076791	Vishay	Vishay
376S00227	376S00203		ALL	rdar://problem/59076791	Fairchild	Vishay
376S00228	376S1179		ALL	rdar://problem/59077240	On Semi	Vishay
376S00007	376S1179		ALL	rdar://problem/59077240	AOS	Vishay
376S00303	376S00012		ALL	rdar://problem/59077463	Diodes Inc	TI
376S1147	376S00281		ALL	rdar://problem/59077684	On Semi	AOS
107S00071	107S00053		ALL	rdar://problem/59078523	Yageo	Cyntec
107S00029	107S00087		ALL	rdar://problem/59081345	TFT	Yageo
138S00332	138S00328		ALL	rdar://problem/59112527	Kyocera	Murata
138S00047	138S00073		ALL	rdar://problem/59118124	Taiyo	Murata
138S0863	138S0853		ALL	rdar://problem/59118514	Taiyo	Murata
138S00077	138S00035		ALL	rdar://problem/59119189	Taiyo	Murata
138S00093	138S00035		ALL	rdar://problem/59119189	Kyocera	Murata
138S00116	138S00071		ALL	rdar://problem/59119528	Taiyo	Murata
138S00117	138S00071		ALL	rdar://problem/59119528	Kyocera	Murata
138S00229	138S00107		ALL	rdar://problem/59123589	Kyocera	Murata
138S00022	138S0891		ALL	rdar://problem/59124126	Taiyo	Murata
152S00398	152S00204		ALL	rdar://problem/59129606	Taiyo	Cyntec
152S00963	152S00885		ALL	rdar://problem/59129928	Taiyo	Cyntec
152S00343	152S00839		ALL	rdar://problem/59130255	Murata	Cyntec
152S01317	152S01268		ALL	rdar://problem/59130415	Taiyo	Cyntec
152S00997	152S00476		ALL	rdar://problem/59130875	Chilisin	Murata
152S01090	152S01085		ALL	rdar://problem/59131117	Chilisin	Murata
107S00055	107S00090		ALL	rdar://problem/59082308	Cyntec	TFT
107S00365	107S00373		ALL	rdar://problem/59081538	Cyntec	TFT
152S01344	152S00883		ALL	rdar://problem/59353109	Chilisin	Cyntec
152S00979	152S00874		ALL	rdar://problem/59364196	Taiyo	Cyntec
197S00046	197S00036		ALL	rdar://problem/59408673	Epson	TXC
197S00047	197S00036		ALL	rdar://problem/59408673	Kyocera	TXC
197S00048	197S00036		ALL	rdar://problem/59408673	Murata	TXC
138S00181	138S0835		ALL	rdar://problem/59408752	Samsung	Murata
138S00291	138S0835		ALL	rdar://problem/59408752	Kyocera	Murata
377S00166	377S00160		ALL	rdar://problem/59407974	Semtech	On Semi
138S00330	138S00081		ALL	rdar://problem/59408911	SEMCO	Murata
740S0118	740S00028		ALL	rdar://problem/59408586	Polytronics	Bussmann
377S00123	377S00031		ALL	rdar://problem/59407768	Semtech	On Semi
377S00186	377S00060		ALL	rdar://problem/59407847	Semtech	ST Micro

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	Alternate Vendor	Primary Vendor
371S00220	371S00181		ALL	rdar://problem/59404055	On Semi	Diodes Inc
371S00085	371S00190		ALL	rdar://problem/59404601	On Semi	Diodes Inc
353S00852	353S4262		ALL	rdar://problem/59403423	On Semi	Diodes Inc
311S00156	311S00129		ALL	rdar://problem/59489090	Nexperia	TI
376S1080	376S0820		ALL	rdar://problem/59489026	Diodes Inc	On Semi
138S00049	138S0831		ALL	rdar://problem/59488798	Kyocera	Murata
311S00269	311S00234		ALL	rdar://problem/59489341	Nexperia	TI
311S00176	311S00153		ALL	rdar://problem/59489111	Diodes Inc	TI
311S00178	311S00177		ALL	rdar://problem/59489119	On Semi	TI
376S1128	376S00282		ALL	rdar://problem/59489044	Diodes Inc	On Semi
376S00224	376S00282		ALL	rdar://problem/59489044	Nexperia	On Semi
128S00093	128S00009		ALL	rdar://problem/59125761	Tokin/Kemet	Kemet
128S00103	128S00009		ALL	rdar://problem/59125761	Samsung	Kemet
128S00106	128S00009		ALL	rdar://problem/59361958	Tokin/Kemet	Kemet
128S00107	128S00009		ALL	rdar://problem/59361958	Kemet	Kemet
128S00110	128S00009		ALL	rdar://problem/59361958	Samsung	Kemet
376S1137	376S00019		ALL	rdar://problem/59489062	Vishay	Diodes Inc
107S00101	107S00005		ALL	TBD	Yageo	Cyntec
107S00102	107S00017		ALL	TBD	Yageo	Cyntec
107S0276	107S00020		ALL	TBD	Cyntec	TFT
107S00370	107S00371		ALL	TBD	Yageo	Cyntec
107S00372	107S00371		ALL	TBD	Vishay	Cyntec
107S00298	107S0298		ALL	TBD	TDK	Murata
107S0150	107S0208		ALL	TBD	Panasonic	Murata
116S00007	116S00006		ALL	TBD	Vishay	Yageo
132S0409	132S00064		ALL	TBD	Taiyo Yuden	Murata
132S00012	132S0401		ALL	TBD	Murata	Taiyo Yuden
138S00084	138S00060		ALL	TBD	Taiyo Yuden	Murata
138S0758	138S00097		ALL	TBD	Murata	Taiyo Yuden
138S00284	138S00136		ALL	TBD	Kyocera	Murata
138S0852	138S0818		ALL	TBD	Samsung	Murata
138S0789	138S0941		ALL	TBD	Samsung	Murata
155S0275	155S00188		ALL	TBD	Taiyo Yuden	Murata
155S0706	155S0302		ALL	TBD	Taiyo Yuden	Murata
155S0741	155S0361		ALL	TBD	Murata	TDK
155S0823	155S0644		ALL	TBD	TDK and Taiyo	Murata
155S00067	155S0667		ALL	TBD	Taiyo Yuden	Panasonic
155S00190	155S0914		ALL	TBD	Taiyo Yuden	Panasonic
138S0706	138S0739		ALL	rdar://problem/59571431	Murata	Samsung
311S00267	311S00244		ALL	TBD	Nexperia	TI
311S00268	311S00246		ALL	TBD	Nexperia	TI
311S00060	311S0273		ALL	TBD	Diodes Inc	Philips
311S00013	311S0508		ALL	TBD	Diodes Inc	NXP
353S02402	353S1429		ALL	TBD	ON Semi	TI
353S02440	353S3698		ALL	rdar://problem/59682314	ON Semi	TI
740S0144	740S00028		ALL	TBD	Bussman	LittleFuse
138S00343	138S00329		ALL	rdar://problem/60096733	Kyocera	Murata
376S00292	376S1140		ALL	rdar://problem/60290671	Nexperia	Diodes Inc.
740S00081	740S00053		ALL	rdar://problem/60394183	Bourns	AEMI

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EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
	685-00339	COMMON PARTS,MLB,X1757	MLB_COMMON
	685-00377	PARTS,SSDNAND1,MLB,X1757	SSD_2L
PP22	939-08408	PCBA,MLB,DCDC,X1757	DCDC_COMMON,DEV_PARTS_BOM,ALTERNATE,NANDCFG:INTERPOSER,CPU:INTERPOSER
	985-01176	DEV PARTS,MLB,X1757	MLB_DEV
Pxxx	939-10388	PCBA,MLB,MSQ,X1757	CMN_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_512G_HY

SOC (BEST), Hynix and Micron 8GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
PNR5	639-10741	PCBA,MLB,BEST,SOC,HY-8G,SD-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_128G_SD
Q1P6	639-11700	PCBA,MLB,BEST,SOC,HY-8G,TO-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_128G_TO
PNR7	639-10743	PCBA,MLB,BEST,SOC,HY-8G,HY-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_256G_HY
Q1P7	639-11701	PCBA,MLB,BEST,SOC,HY-8G,SD-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_256G_SD
Q1P8	639-11702	PCBA,MLB,BEST,SOC,HY-8G,TO-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_256G_TO
Q1P9	639-11703	PCBA,MLB,BEST,SOC,HY-8G,HY-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_512G_HY
PNR9	639-10745	PCBA,MLB,BEST,SOC,HY-8G,TO-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_512G_TO
Q1PC	639-11704	PCBA,MLB,BEST,SOC,HY-8G,SD-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_1P0T_SD
PNRD	639-10747	PCBA,MLB,BEST,SOC,HY-8G,TO-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_1P0T_TO
PNRG	639-10749	PCBA,MLB,BEST,SOC,HY-8G,HY-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_2P0T_HY
Q1PD	639-11705	PCBA,MLB,BEST,SOC,HY-8G,TO-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_BEST,NANDCFG:ITLC_S5E_2P0T_TO

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
PVD4	639-10924	PCBA,MLB,BEST,SOC,MI-8G,SD-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_128G_SD
Q1PF	639-11706	PCBA,MLB,BEST,SOC,MI-8G,TO-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_128G_TO
PVD6	639-10926	PCBA,MLB,BEST,SOC,MI-8G,HY-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_256G_HY
Q1PG	639-11707	PCBA,MLB,BEST,SOC,MI-8G,SD-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_256G_SD
Q1PH	639-11708	PCBA,MLB,BEST,SOC,MI-8G,TO-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_256G_TO
Q1PJ	639-11709	PCBA,MLB,BEST,SOC,MI-8G,HY-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_512G_HY
Q1PK	639-11710	PCBA,MLB,BEST,SOC,MI-8G,TO-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_512G_TO
Q1PL	639-11711	PCBA,MLB,BEST,SOC,MI-8G,SD-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_1P0T_SD
Q1PM	639-11712	PCBA,MLB,BEST,SOC,MI-8G,TO-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_1P0T_TO
Q1PN	639-11713	PCBA,MLB,BEST,SOC,MI-8G,HY-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_2P0T_HY
Q1PP	639-11714	PCBA,MLB,BEST,SOC,MI-8G,TO-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_BEST,NANDCFG:ITLC_S5E_2P0T_TO

SOC (GOOD), Hynix and Micron 8GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
Q2D9	639-11752	PCBA,MLB,GOOD,SOC,HY-8G,SD-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_128G_SD,SOC_SEL:GOOD
Q2DC	639-11753	PCBA,MLB,GOOD,SOC,HY-8G,TO-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_128G_TO,SOC_SEL:GOOD
Q2DD	639-11754	PCBA,MLB,GOOD,SOC,HY-8G,HY-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_256G_HY,SOC_SEL:GOOD
Q2DF	639-11755	PCBA,MLB,GOOD,SOC,HY-8G,SD-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_256G_SD,SOC_SEL:GOOD
Q2DG	639-11756	PCBA,MLB,GOOD,SOC,HY-8G,TO-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_256G_TO,SOC_SEL:GOOD
Q2DH	639-11757	PCBA,MLB,GOOD,SOC,HY-8G,HY-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_512G_HY,SOC_SEL:GOOD
Q2DJ	639-11758	PCBA,MLB,GOOD,SOC,HY-8G,TO-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_512G_TO,SOC_SEL:GOOD
Q2DK	639-11759	PCBA,MLB,GOOD,SOC,HY-8G,SD-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_1P0T_SD,SOC_SEL:GOOD
Q2DL	639-11760	PCBA,MLB,GOOD,SOC,HY-8G,TO-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_1P0T_TO,SOC_SEL:GOOD
Q2DM	639-11761	PCBA,MLB,GOOD,SOC,HY-8G,HY-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_2P0T_HY,SOC_SEL:GOOD
Q2DN	639-11762	PCBA,MLB,GOOD,SOC,HY-8G,TO-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_8GB_GOOD,NANDCFG:ITLC_S5E_2P0T_TO,SOC_SEL:GOOD

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
Q2DP	639-11763	PCBA,MLB,GOOD,SOC,MI-8G,SD-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_128G_SD,SOC_SEL:GOOD
Q2DQ	639-11764	PCBA,MLB,GOOD,SOC,MI-8G,TO-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_128G_TO,SOC_SEL:GOOD
Q2DR	639-11765	PCBA,MLB,GOOD,SOC,MI-8G,HY-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_256G_HY,SOC_SEL:GOOD
Q2DT	639-11766	PCBA,MLB,GOOD,SOC,MI-8G,SD-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_256G_SD,SOC_SEL:GOOD
Q2DV	639-11767	PCBA,MLB,GOOD,SOC,MI-8G,TO-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_256G_TO,SOC_SEL:GOOD
Q2DW	639-11768	PCBA,MLB,GOOD,SOC,MI-8G,HY-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_512G_HY,SOC_SEL:GOOD
Q2DX	639-11769	PCBA,MLB,GOOD,SOC,MI-8G,TO-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_512G_TO,SOC_SEL:GOOD
Q2DY	639-11770	PCBA,MLB,GOOD,SOC,MI-8G,SD-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_1P0T_SD,SOC_SEL:GOOD
Q2F0	639-11771	PCBA,MLB,GOOD,SOC,MI-8G,TO-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_1P0T_TO,SOC_SEL:GOOD
Q2F1	639-11772	PCBA,MLB,GOOD,SOC,MI-8G,HY-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_2P0T_HY,SOC_SEL:GOOD
Q2F2	639-11773	PCBA,MLB,GOOD,SOC,MI-8G,TO-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_8GB_GOOD,NANDCFG:ITLC_S5E_2P0T_TO,SOC_SEL:GOOD

SOC (BEST), Hynix and Micron 16GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
PNR6	639-10742	PCBA,MLB,BEST,SOC,HY-16G,SD-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_128G_SD
Q1PQ	639-11715	PCBA,MLB,BEST,SOC,HY-16G,TO-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_128G_TO
PNR8	639-10744	PCBA,MLB,BEST,SOC,HY-16G,HY-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_256G_HY
Q1PR	639-11716	PCBA,MLB,BEST,SOC,HY-16G,SD-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_256G_SD
Q1PT	639-11717	PCBA,MLB,BEST,SOC,HY-16G,TO-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_256G_TO
Q1PV	639-11718	PCBA,MLB,BEST,SOC,HY-16G,HY-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_512G_HY
PNRC	639-10746	PCBA,MLB,BEST,SOC,HY-16G,TO-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_512G_TO
Q1PW	639-11719	PCBA,MLB,BEST,SOC,HY-16G,SD-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_1P0T_SD
PNRF	639-10748	PCBA,MLB,BEST,SOC,HY-16G,TO-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_1P0T_TO
PNRH	639-10750	PCBA,MLB,BEST,SOC,HY-16G,HY-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_2P0T_HY
Q1PX	639-11720	PCBA,MLB,BEST,SOC,HY-16G,TO-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_BEST,NANDCFG:ITLC_S5E_2P0T_TO

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
PVD5	639-10925	PCBA,MLB,BEST,SOC,MI-16G,SD-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_128G_SD
Q1PY	639-11721	PCBA,MLB,BEST,SOC,MI-16G,TO-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_128G_TO
PVD7	639-10927	PCBA,MLB,BEST,SOC,MI-16G,HY-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_256G_HY
Q1Q0	639-11722	PCBA,MLB,BEST,SOC,MI-16G,SD-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_256G_SD
Q1Q1	639-11723	PCBA,MLB,BEST,SOC,MI-16G,TO-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_256G_TO
Q1Q2	639-11724	PCBA,MLB,BEST,SOC,MI-16G,HY-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_512G_HY
Q1Q3	639-11725	PCBA,MLB,BEST,SOC,MI-16G,TO-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_512G_TO
Q1Q4	639-11726	PCBA,MLB,BEST,SOC,MI-16G,SD-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_1P0T_SD
Q1Q5	639-11727	PCBA,MLB,BEST,SOC,MI-16G,TO-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_1P0T_TO
Q1Q6	639-11728	PCBA,MLB,BEST,SOC,MI-16G,HY-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_2P0T_HY
Q1Q7	639-11729	PCBA,MLB,BEST,SOC,MI-16G,TO-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_BEST,NANDCFG:ITLC_S5E_2P0T_TO

SOC (GOOD), Hynix and Micron 16GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
Q2F3	639-11774	PCBA,MLB,GOOD,SOC,HY-16G,SD-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_128G_SD,SOC_SEL:GOOD
Q2F4	639-11775	PCBA,MLB,GOOD,SOC,HY-16G,TO-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_128G_TO,SOC_SEL:GOOD
Q2F5	639-11776	PCBA,MLB,GOOD,SOC,HY-16G,HY-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_256G_HY,SOC_SEL:GOOD
Q2F6	639-11777	PCBA,MLB,GOOD,SOC,HY-16G,SD-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_256G_SD,SOC_SEL:GOOD
Q2F7	639-11778	PCBA,MLB,GOOD,SOC,HY-16G,TO-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_256G_TO,SOC_SEL:GOOD
Q2F8	639-11779	PCBA,MLB,GOOD,SOC,HY-16G,HY-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_512G_HY,SOC_SEL:GOOD
Q2F9	639-11780	PCBA,MLB,GOOD,SOC,HY-16G,TO-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_512G_TO,SOC_SEL:GOOD
Q2FC	639-11781	PCBA,MLB,GOOD,SOC,HY-16G,SD-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_1P0T_SD,SOC_SEL:GOOD
Q2FD	639-11782	PCBA,MLB,GOOD,SOC,HY-16G,TO-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_1P0T_TO,SOC_SEL:GOOD
Q2FF	639-11783	PCBA,MLB,GOOD,SOC,HY-16G,HY-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_2P0T_HY,SOC_SEL:GOOD
Q2FG	639-11784	PCBA,MLB,GOOD,SOC,HY-16G,TO-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_HYNIX_16GB_GOOD,NANDCFG:ITLC_S5E_2P0T_TO,SOC_SEL:GOOD

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
Q2FH	639-11785	PCBA,MLB,GOOD,SOC,MI-16G,SD-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_128G_SD,SOC_SEL:GOOD
Q2FJ	639-11786	PCBA,MLB,GOOD,SOC,MI-16G,TO-128G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_128G_TO,SOC_SEL:GOOD
Q2FK	639-11787	PCBA,MLB,GOOD,SOC,MI-16G,HY-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_256G_HY,SOC_SEL:GOOD
Q2FL	639-11788	PCBA,MLB,GOOD,SOC,MI-16G,SD-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_256G_SD,SOC_SEL:GOOD
Q2FM	639-11789	PCBA,MLB,GOOD,SOC,MI-16G,TO-256G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_256G_TO,SOC_SEL:GOOD
Q2FN	639-11790	PCBA,MLB,GOOD,SOC,MI-16G,HY-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_512G_HY,SOC_SEL:GOOD
Q2FP	639-11791	PCBA,MLB,GOOD,SOC,MI-16G,TO-512G,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_512G_TO,SOC_SEL:GOOD
Q2FQ	639-11792	PCBA,MLB,GOOD,SOC,MI-16G,SD-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_1P0T_SD,SOC_SEL:GOOD
Q2FR	639-11793	PCBA,MLB,GOOD,SOC,MI-16G,TO-1P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_1P0T_TO,SOC_SEL:GOOD
Q2FT	639-11794	PCBA,MLB,GOOD,SOC,MI-16G,HY-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_2P0T_HY,SOC_SEL:GOOD
Q2FV	639-11795	PCBA,MLB,GOOD,SOC,MI-16G,TO-2P0T,X1757	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE,CPU:SOC_MICRON_16GB_GOOD,NANDCFG:ITLC_S5E_2P0T_TO,SOC_SEL:GOOD

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